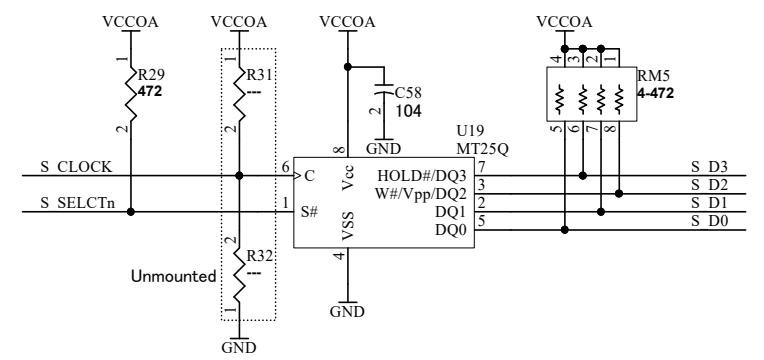
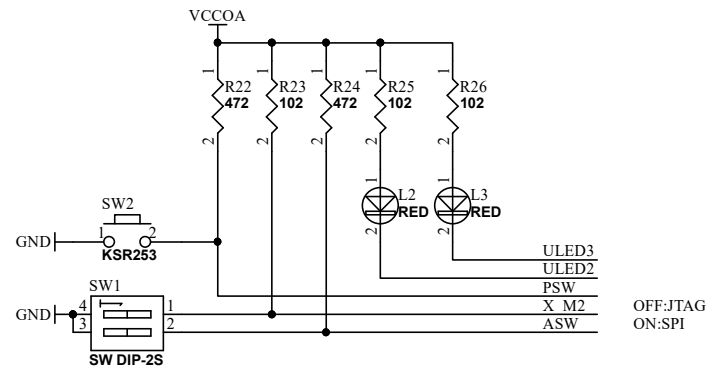
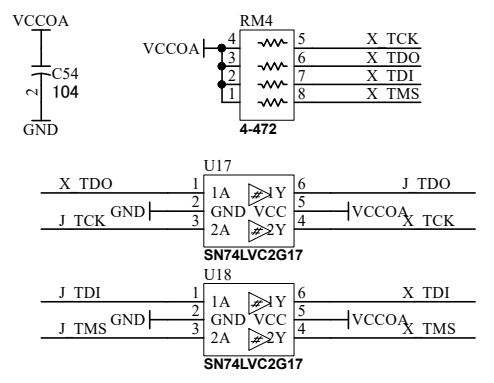
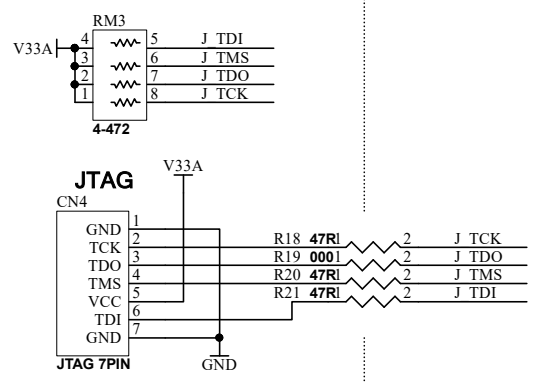
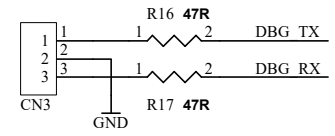
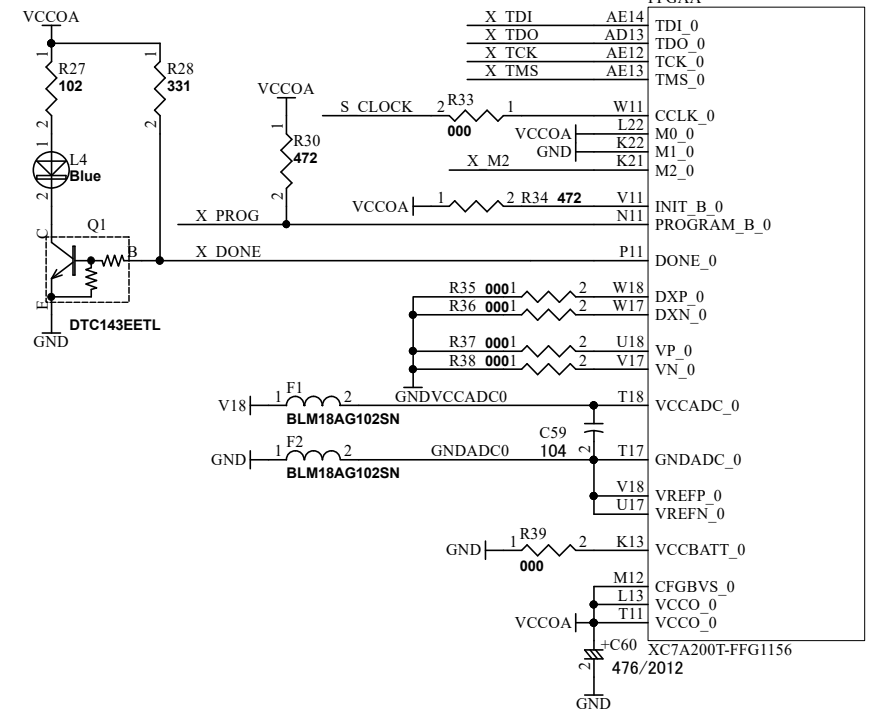
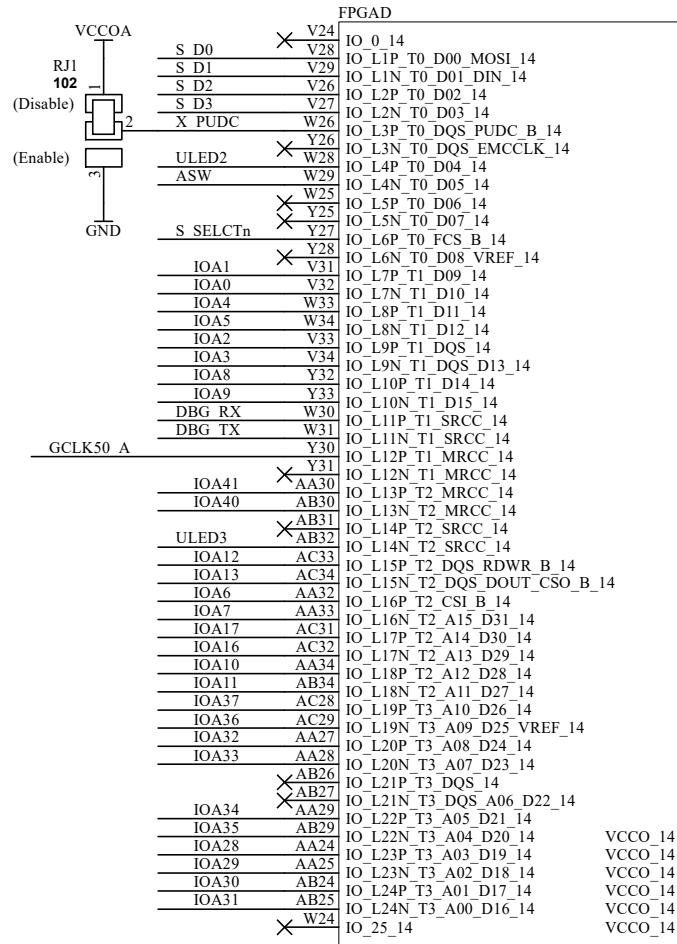
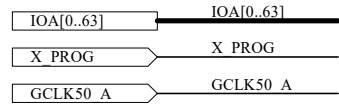


XCM211R1-SCH-A.pdf

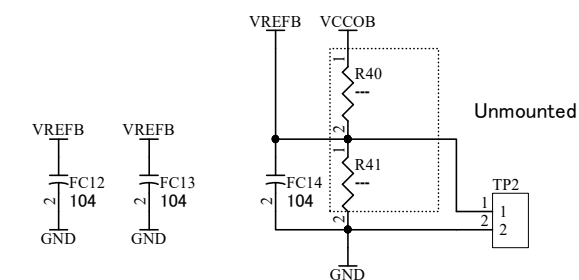
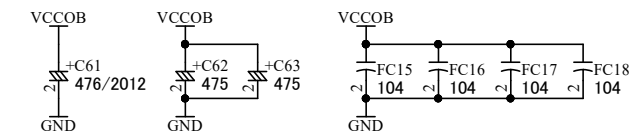
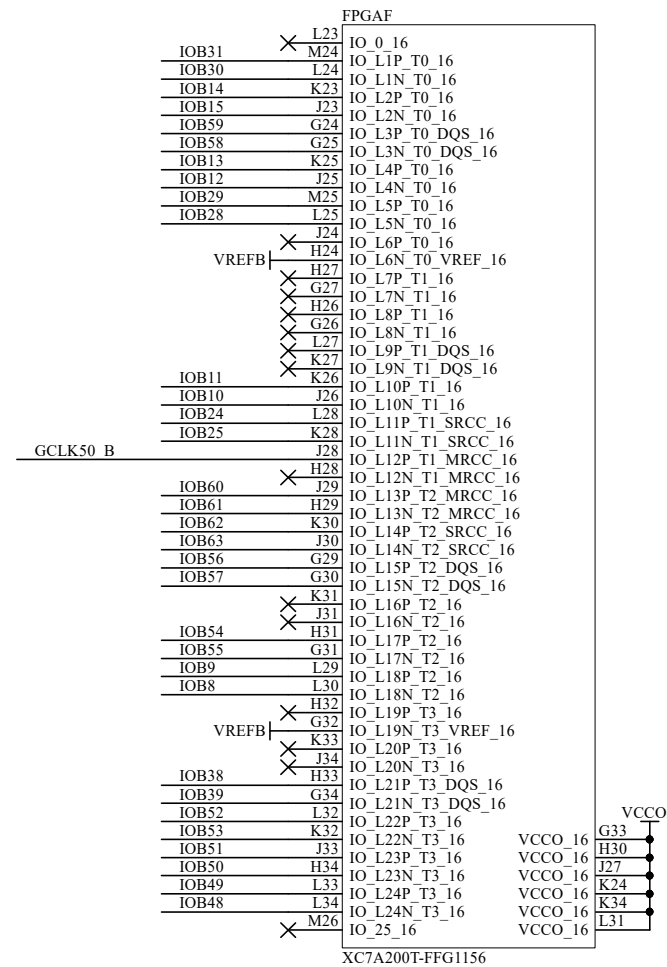
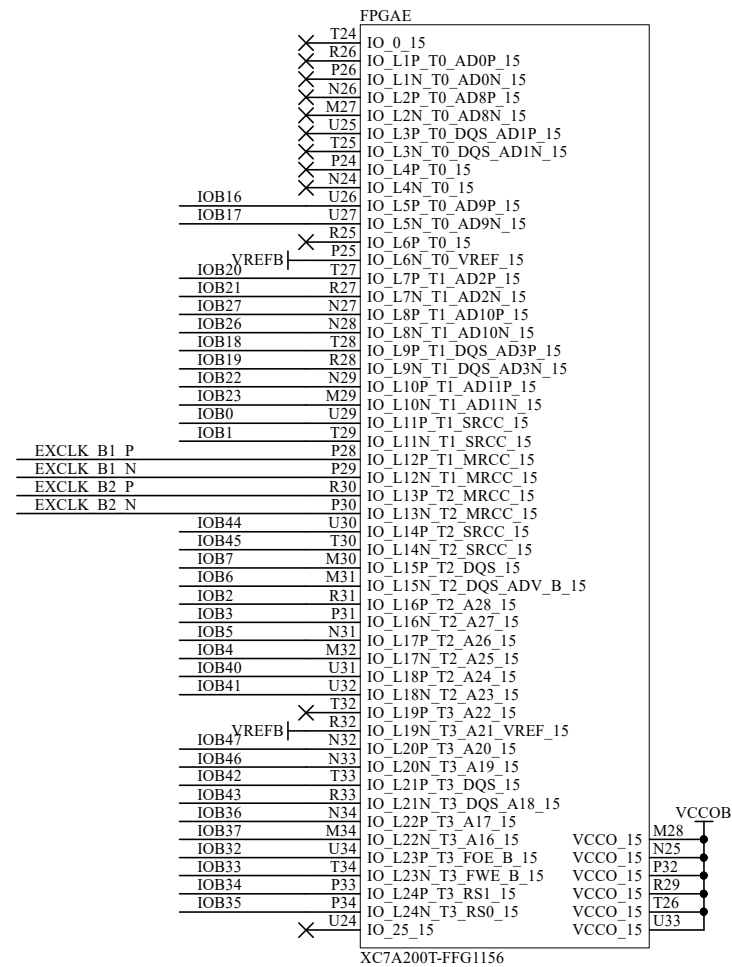


DSN:	TITLE: ARTIX-7 FFG1156 FPGA Board
DOC. No:	<b>XCM-211</b>
FILE: XCM211.SchDoc	DATE: 2018/06/04 13:25:56
Sheet:	1 / 8



DSN:	TITLE: ARTIX-7 FFG1156 FPGA Board
DOC. No:	XCM-211
FILE: IOA_CONFIG.SchDoc	DATE: 2018/06/04 13:25:56
Sheet: 2 / 8	

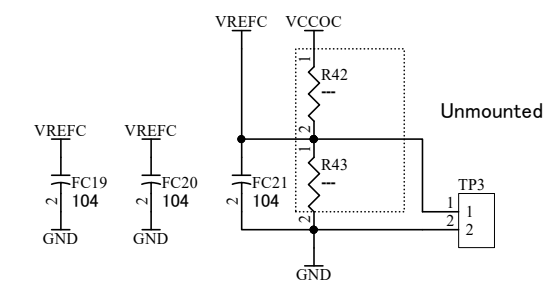
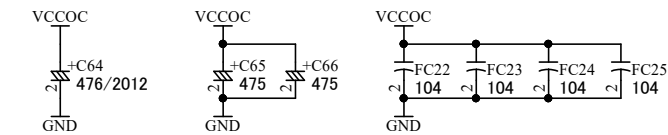
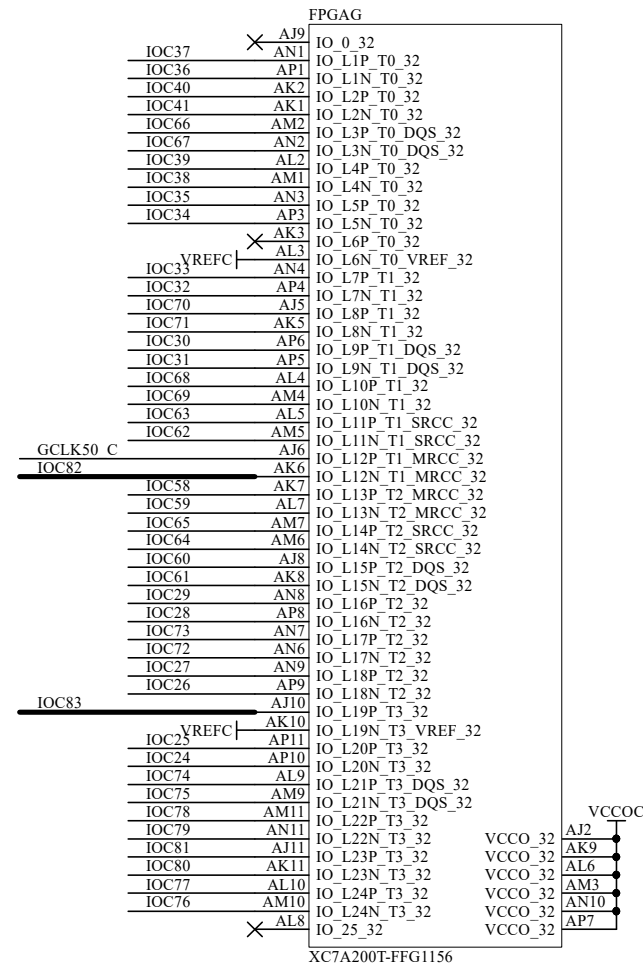
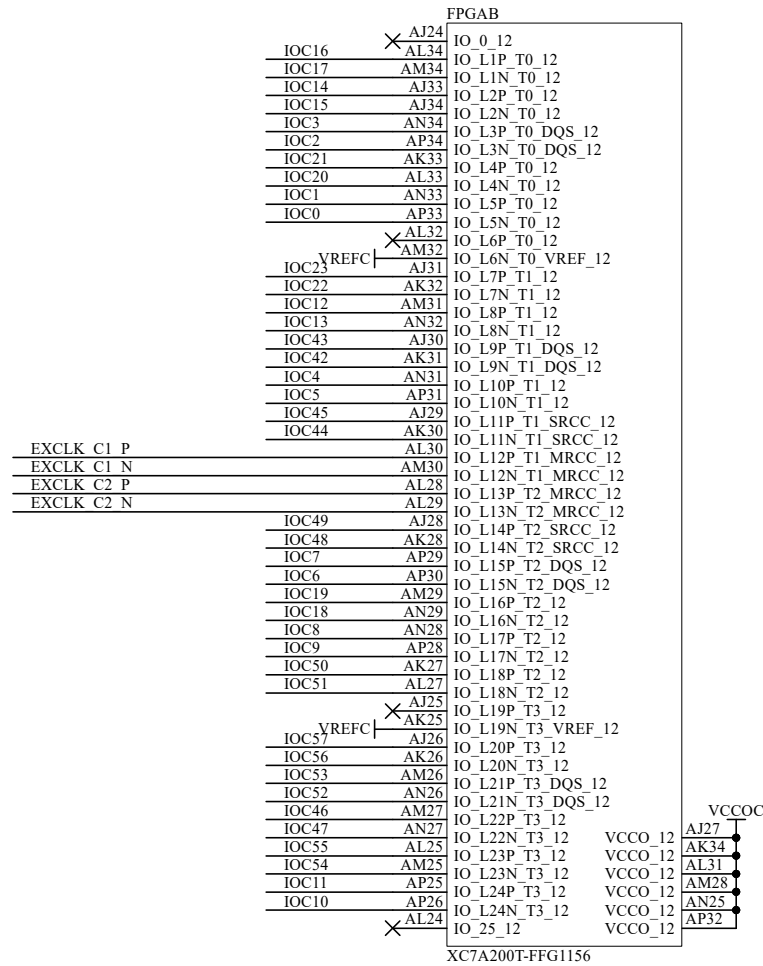
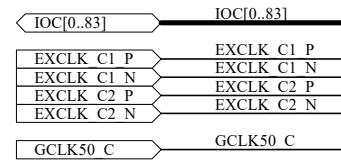
IOB[0..63]	IOB[0..63]
EXCLK B1 P	EXCLK B1 P
EXCLK B1 N	EXCLK B1 N
EXCLK B2 P	EXCLK B2 P
EXCLK B2 N	EXCLK B2 N
GCLK50 B	GCLK50 B



XCM211R1-SCH-A.pdf



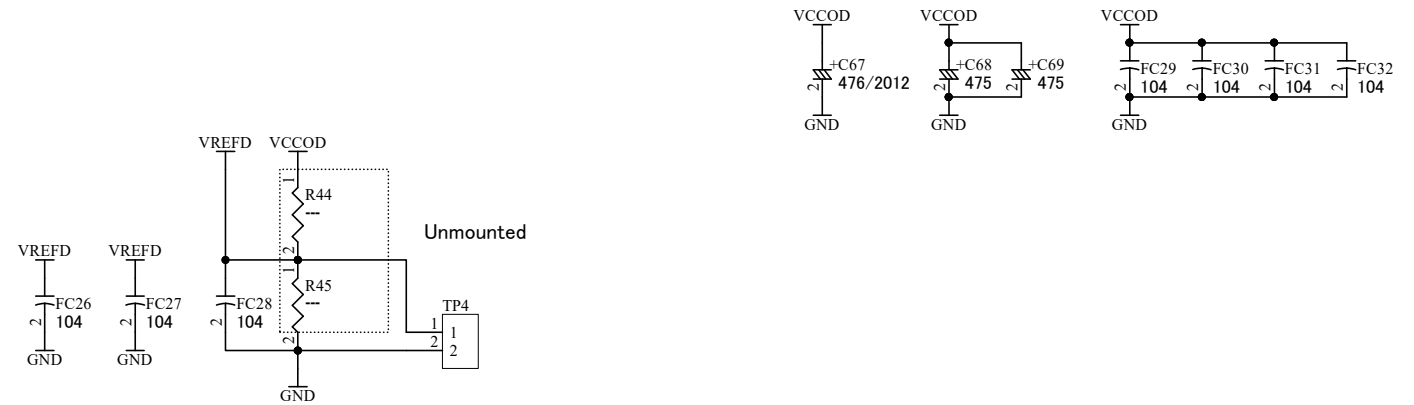
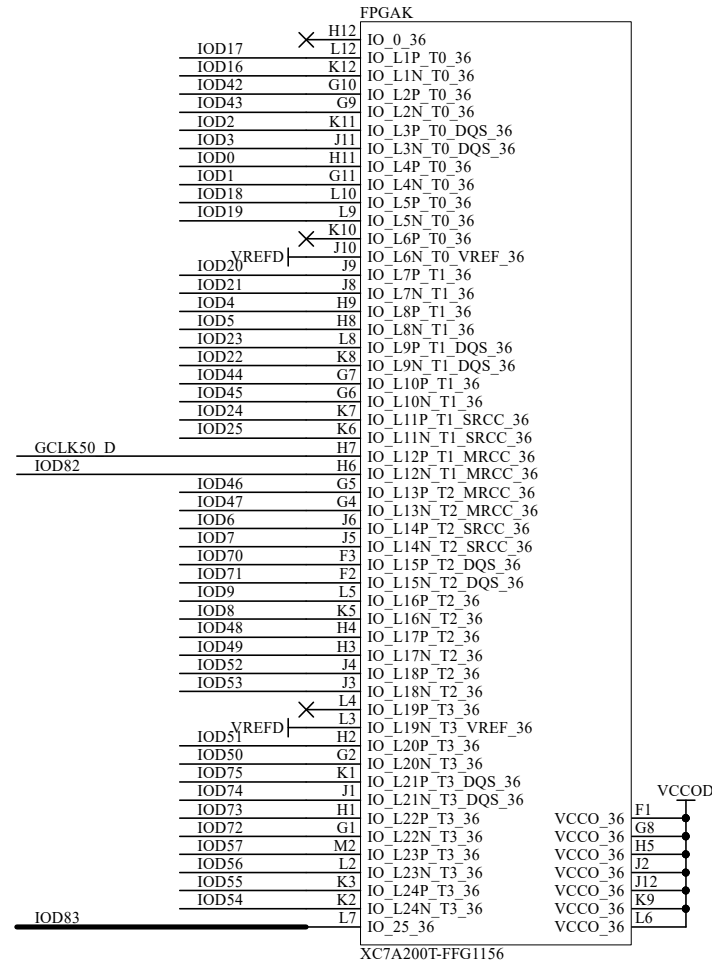
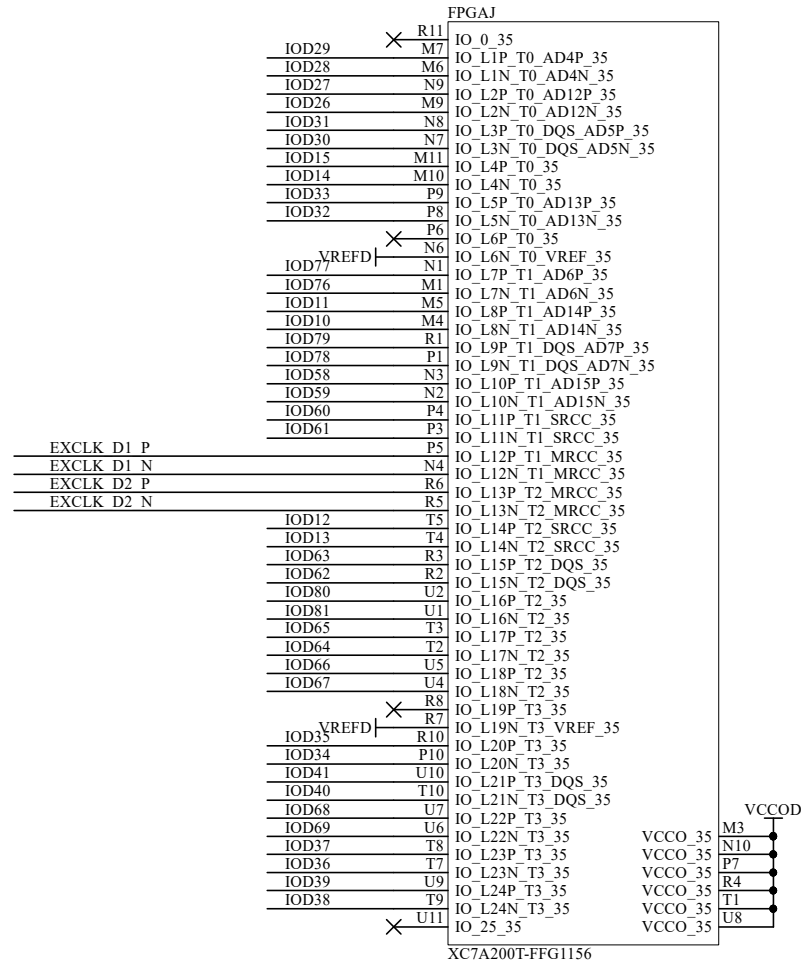
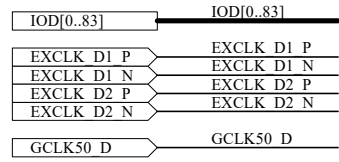
DSN:	TITLE: ARTIX-7 FFG1156 FPGA Board
DOC. No:	<b>XCM-211</b>
FILE: IOB.SchDoc	DATE: 2018/06/04 13:25:56
Sheet: 3 / 8	A



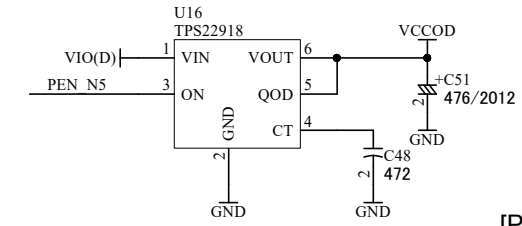
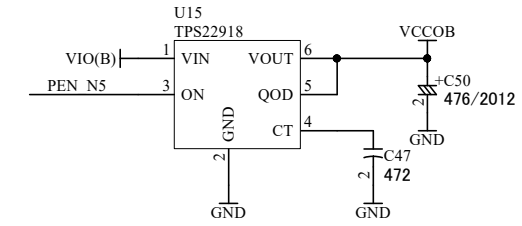
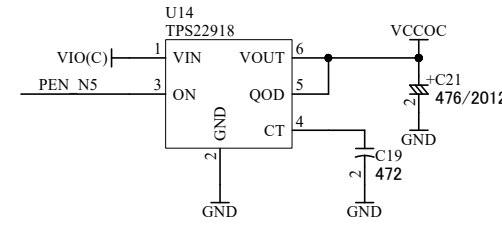
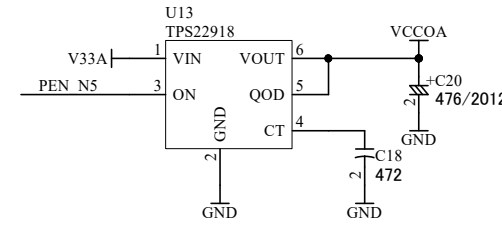
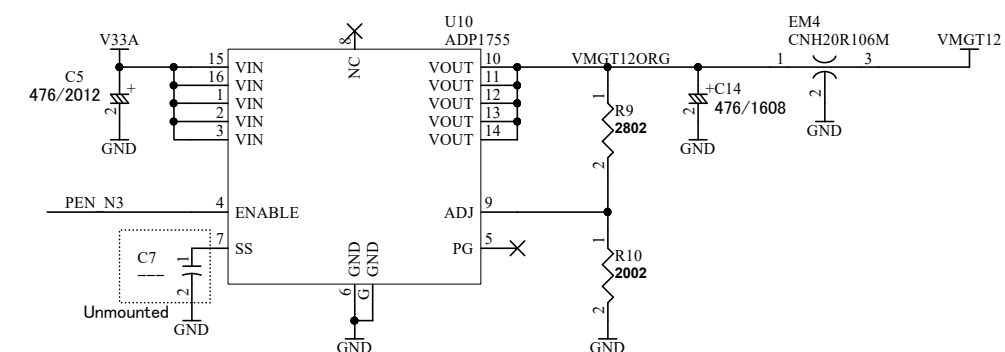
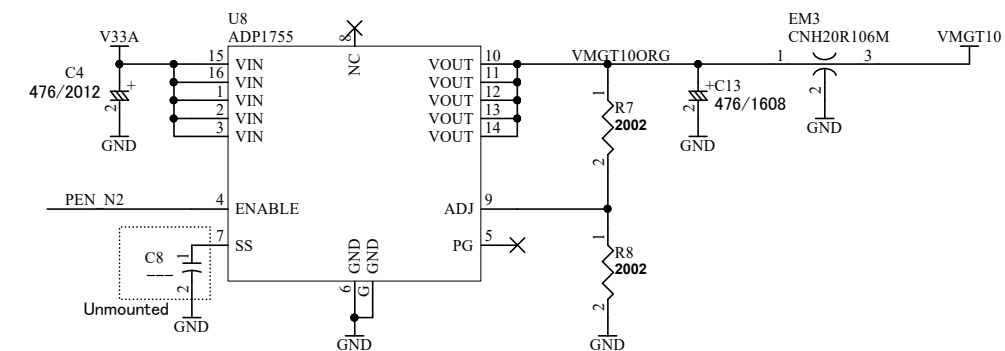
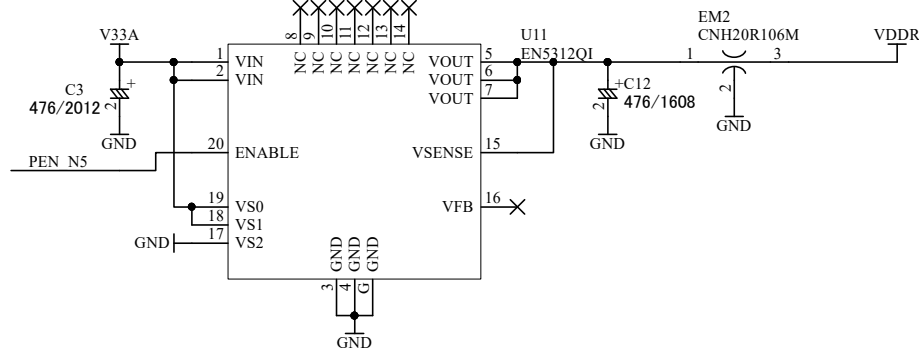
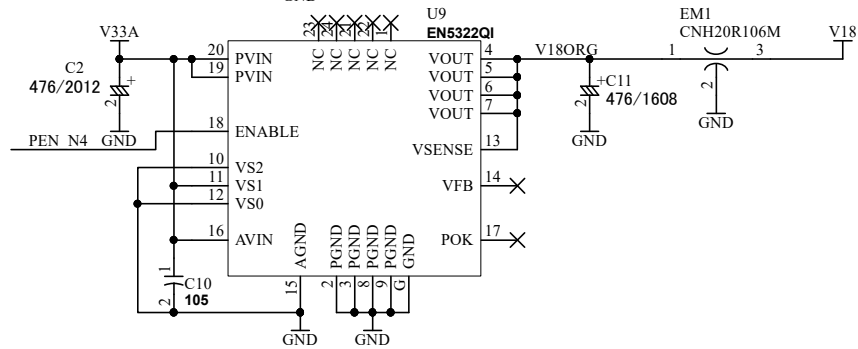
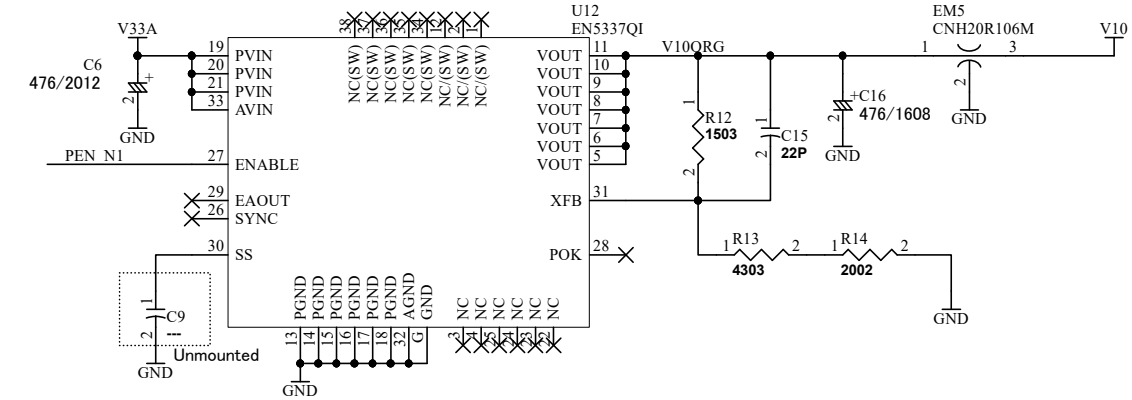
XCM211R1-SCH-A.pdf



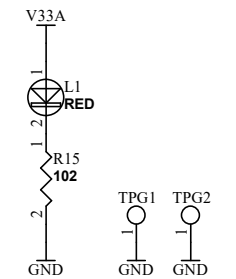
DSN:	TITLE: ARTIX-7 FFG1156 FPGA Board
DOC. No:	<b>XCM-211</b>
FILE: IOC.SchDoc	DATE: 2018/06/04 13:25:56
Sheet:	<b>A</b>
V5.20150107	



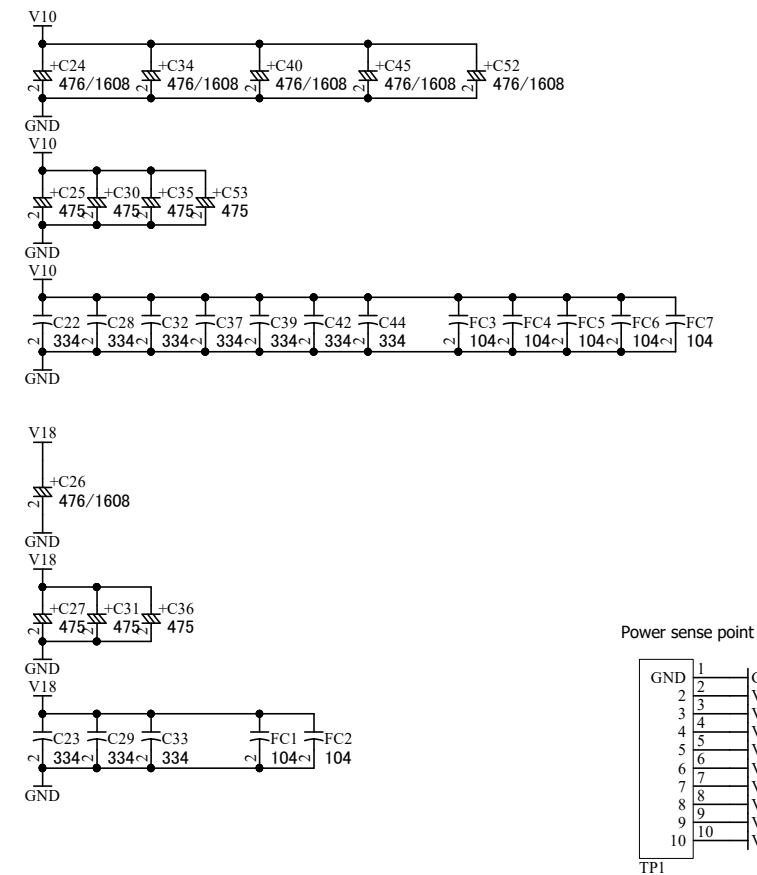
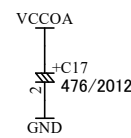
PEN N1	PEN N1
PEN N2	PEN N2
PEN N3	PEN N3
PEN N4	PEN N4
PEN N5	PEN N5



[POWER]



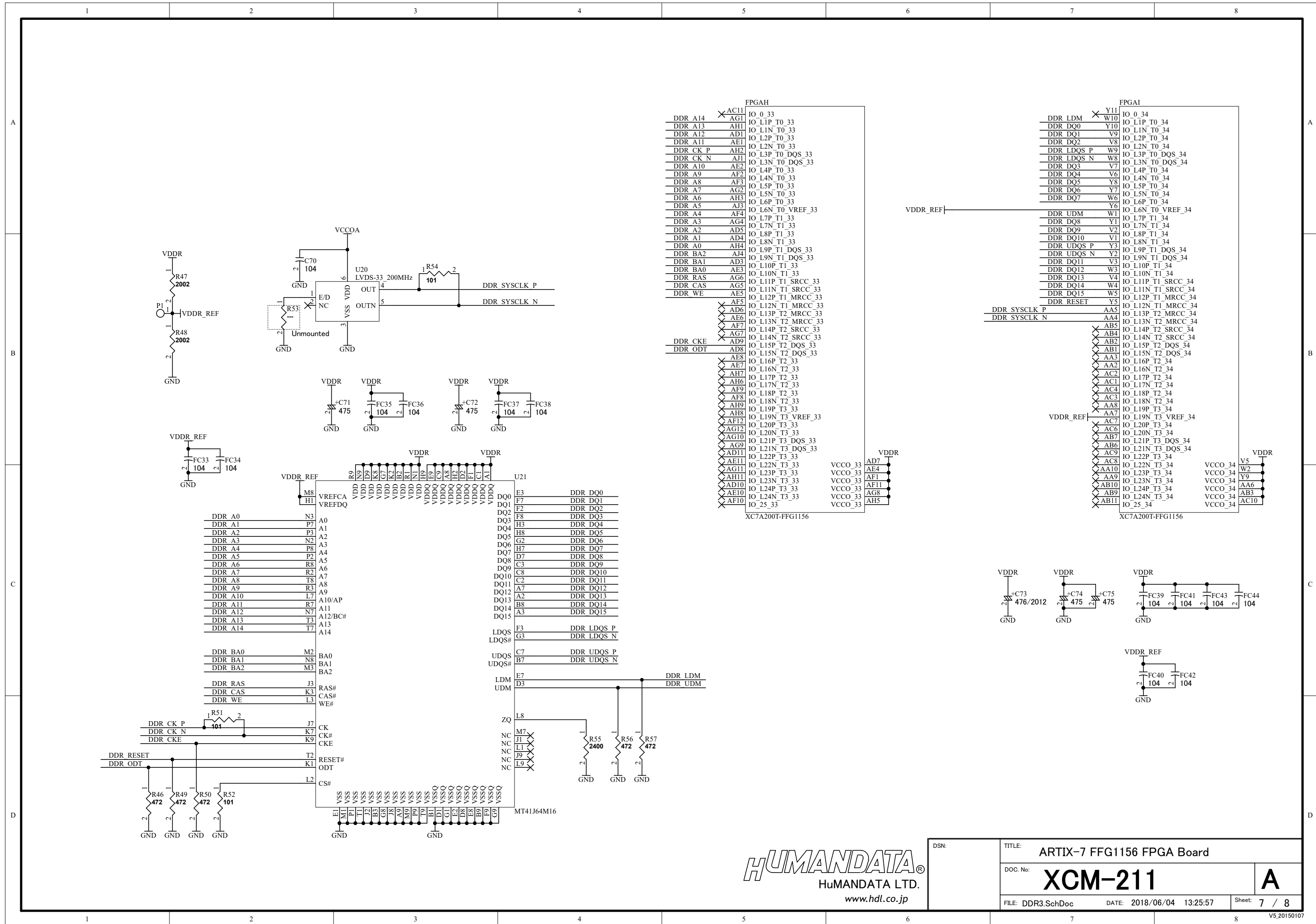
FPGA		K14	
M22	VCCAUX	K16	V10
N13	VCCAUX	K18	V10
N23	VCCAUX	K20	V10
P12	VCCAUX	L15	V10
P22	VCCAUX	L17	V10
R13	VCCAUX	L19	V10
T12	VCCAUX	M14	V10
T22	VCCAUX	M16	V10
U13	VCCAUX	M18	V10
V12	VCCAUX	N15	V10
V22	VCCAUX	N17	V10
W13	VCCAUX	N19	V10
W23	VCCAUX	P14	V10
Y12	VCCAUX	P16	V10
Y22	VCCAUX	P18	V10
AA13	VCCAUX	R15	V10
AA23	VCCAUX	R17	V10
AB12	VCCAUX	R19	V10
AB22	VCCAUX	T14	V10
AC13	VCCAUX	T16	V10
AC23	VCCAUX	U15	V10
AD12	VCCAUX	U19	V10
M20	VCCBRAM	V16	V10
N21	VCCBRAM	W15	V10
P20	VCCBRAM	W19	V10
R21	VCCBRAM	Y14	V10
T20	VCCBRAM	Y16	V10
U21	VCCBRAM	Y18	V10
V20	VCCBRAM	AA15	V10
W21	VCCBRAM	AA17	V10
Y20	VCCBRAM	AA19	V10
AA21	VCCBRAM	AB14	V10
AB20	VCCBRAM	AB16	V10
AC21	VCCBRAM	AB18	V10
A31	VCCO_17	AC15	V10
B28	VCCO_17	AC17	V10
C25	VCCO_17	AC19	V10
D32	VCCO_17	AD14	V10
E29	VCCO_17	AD16	V10
F26	VCCO_17	AD18	V10
A6	VCCO_17	AD20	V10
B3	VCCO_37	AD22	V10
C10	VCCO_37	AE15	V10
D7	VCCO_37	AE17	V10
E4	VCCO_37	AE19	V10
F11	VCCO_37	AE21	V10



XCM211R1-SCH-A.pdf

**HUMAN DATA**  
HuMANDATA LTD.  
www.hdl.co.jp

DSN:	TITLE: ARTIX-7 FFG1156 FPGA Board
DOC. No:	<b>XCM-211</b>
FILE: POWER.SchDoc	DATE: 2018/06/04 13:25:56
Sheet: 6 / 8	<b>A</b>



FPGA I/O Connections (XC7A200T-FFG1156)

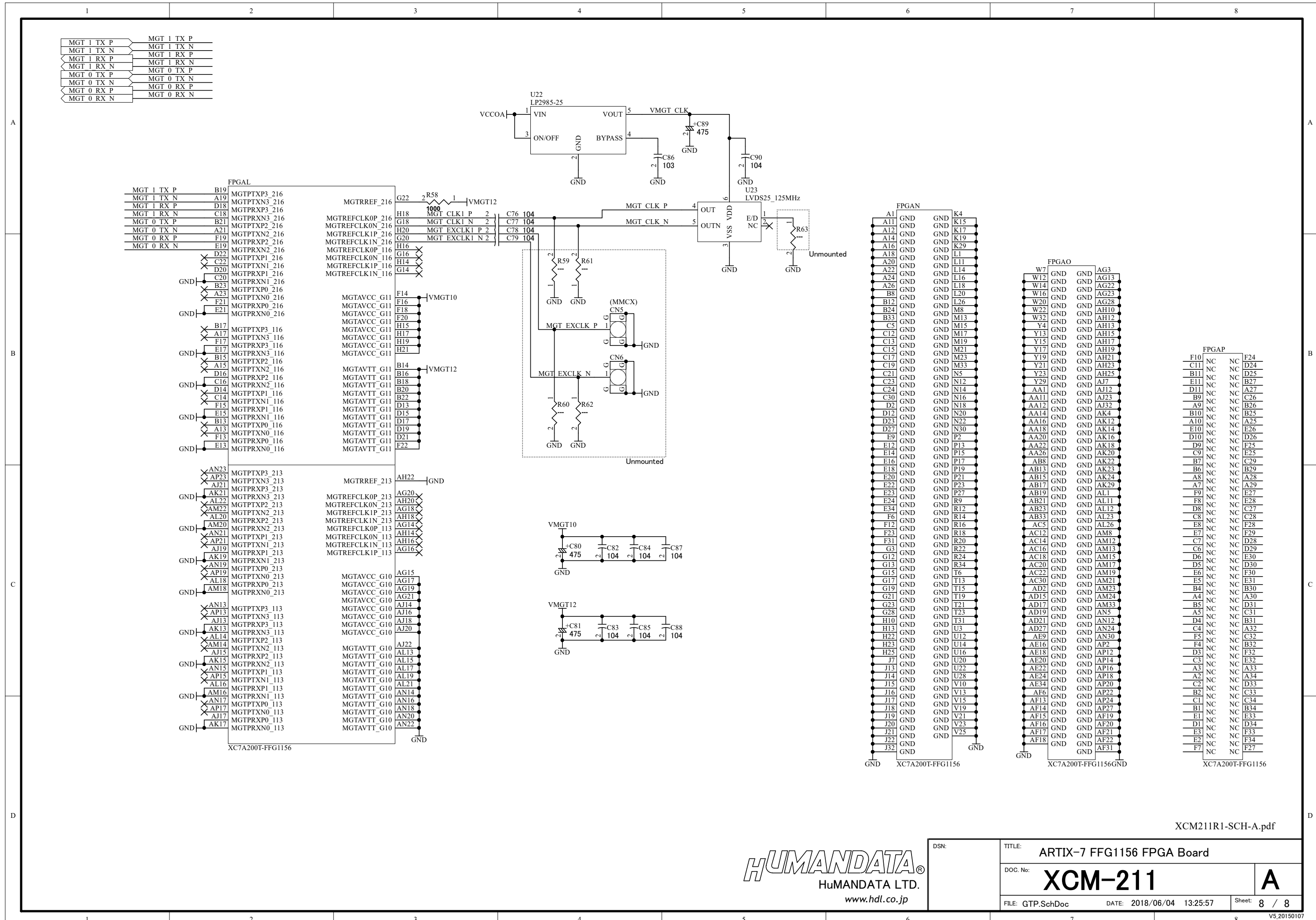
Signal	FPGA Pin	Board Pin
DDR A14	AC11	IO_0_33
DDR A13	AG1	IO_L1P_T0_33
DDR A12	AH1	IO_L1N_T0_33
DDR A11	AD1	IO_L2P_T0_33
DDR A10	AE1	IO_L2N_T0_33
DDR CK P	AH2	IO_L3P_T0_DQS_33
DDR CK N	AJ1	IO_L3N_T0_DQS_33
DDR A9	AF2	IO_L4P_T0_33
DDR A8	AF3	IO_L4N_T0_33
DDR A7	AG2	IO_L5P_T0_33
DDR A6	AH3	IO_L5N_T0_33
DDR A5	AJ3	IO_L6P_T0_33
DDR A4	AF4	IO_L6N_T0_VREF_33
DDR A3	AG4	IO_L7P_T1_33
DDR A2	AD5	IO_L7N_T1_33
DDR A1	AD4	IO_L8P_T1_33
DDR A0	AH4	IO_L8N_T1_33
DDR BA2	AJ4	IO_L9P_T1_DQS_33
DDR BA1	AD3	IO_L9N_T1_DQS_33
DDR BA0	AE3	IO_L10P_T1_33
DDR RAS	AG6	IO_L10N_T1_33
DDR CAS	AG5	IO_L11P_T1_SRCC_33
DDR WE	AE5	IO_L11N_T1_SRCC_33
DDR CKE	AF5	IO_L12P_T1_MRCC_33
DDR ODT	AD6	IO_L13P_T2_MRCC_33
	AE6	IO_L13N_T2_MRCC_33
	AF7	IO_L14P_T2_SRCC_33
	AG7	IO_L14N_T2_SRCC_33
	AD9	IO_L15P_T2_DQS_33
	AD8	IO_L15N_T2_DQS_33
	AE8	IO_L16P_T2_33
	AH7	IO_L16N_T2_33
	AH6	IO_L17P_T2_33
	AF9	IO_L17N_T2_33
	AF8	IO_L18P_T2_33
	AH9	IO_L18N_T2_33
	AH8	IO_L19P_T3_VREF_33
	AF12	IO_L20P_T3_33
	AG12	IO_L20N_T3_33
	AG10	IO_L21P_T3_DQS_33
	AG9	IO_L21N_T3_DQS_33
	AD11	IO_L22P_T3_33
	AE11	IO_L22N_T3_33
	AG11	IO_L23P_T3_33
	AH11	IO_L23N_T3_33
	AD10	IO_L24P_T3_33
	AE10	IO_L24N_T3_33
	AF10	IO_25_33

FPGA I/O Connections (XC7A200T-FFG1156)

Signal	FPGA Pin	Board Pin
DDR LDM	Y11	IO_0_34
DDR DQ0	Y10	IO_L1P_T0_34
DDR DQ1	V9	IO_L1N_T0_34
DDR DQ2	V8	IO_L2P_T0_34
DDR LDQS P	W9	IO_L2N_T0_34
DDR LDQS N	W8	IO_L3P_T0_DQS_34
DDR DQ3	V7	IO_L3N_T0_DQS_34
DDR DQ4	V6	IO_L4P_T0_34
DDR DQ5	Y8	IO_L4N_T0_34
DDR DQ6	Y7	IO_L5P_T0_34
DDR DQ7	W6	IO_L5N_T0_34
	Y6	IO_L6P_T0_34
	Y6	IO_L6N_T0_VREF_34
DDR UDM	W1	IO_L7P_T1_34
DDR DQ8	Y1	IO_L7N_T1_34
DDR DQ9	V2	IO_L8P_T1_34
DDR DQ10	V1	IO_L8N_T1_34
DDR UDQS P	Y3	IO_L9P_T1_DQS_34
DDR UDQS N	Y2	IO_L9N_T1_DQS_34
DDR DQ11	V3	IO_L10P_T1_34
DDR DQ12	W3	IO_L10N_T1_34
DDR DQ13	V4	IO_L11P_T1_SRCC_34
DDR DQ14	W4	IO_L11N_T1_SRCC_34
DDR DQ15	W5	IO_L12P_T1_MRCC_34
DDR RESET	Y5	IO_L12N_T1_MRCC_34
DDR SYSCLK P	AA5	IO_L13P_T2_MRCC_34
DDR SYSCLK N	AA4	IO_L13N_T2_MRCC_34
	AB5	IO_L14P_T2_SRCC_34
	AB4	IO_L14N_T2_SRCC_34
	AB2	IO_L15P_T2_DQS_34
	AB1	IO_L15N_T2_DQS_34
	AA3	IO_L16P_T2_34
	AA2	IO_L16N_T2_34
	AC2	IO_L17P_T2_34
	AC1	IO_L17N_T2_34
	AC4	IO_L18P_T2_34
	AC3	IO_L18N_T2_34
	AA8	IO_L19P_T3_34
	AA7	IO_L19N_T3_VREF_34
	AC7	IO_L20P_T3_34
	AC6	IO_L20N_T3_34
	AB7	IO_L21P_T3_DQS_34
	AB6	IO_L21N_T3_DQS_34
	AC9	IO_L22P_T3_34
	AC8	IO_L22N_T3_34
	AA10	IO_L23P_T3_34
	AA9	IO_L23N_T3_34
	AB10	IO_L24P_T3_34
	AB9	IO_L24N_T3_34
	AB11	IO_25_34



DSN:	TITLE: ARTIX-7 FFG1156 FPGA Board
DOC. No:	XCM-211
FILE: DDR3.SchDoc	DATE: 2018/06/04 13:25:57
Sheet: 7 / 8	



DSN:	TITLE: ARTIX-7 FFG1156 FPGA Board
DOC. No:	<b>XCM-211</b>
FILE: GTP.SchDoc	DATE: 2018/06/04 13:25:57
Sheet:	<b>A</b>
8 / 8	