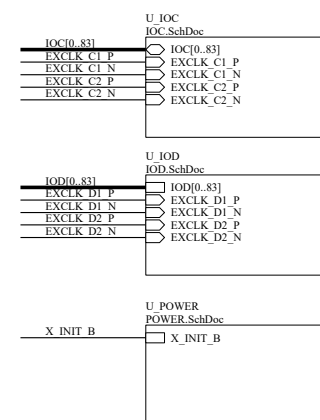
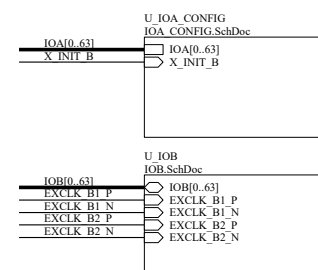
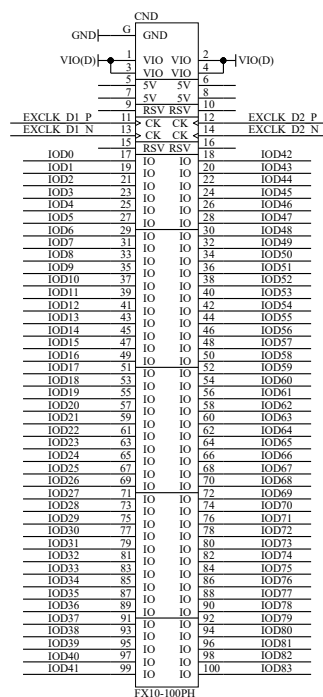
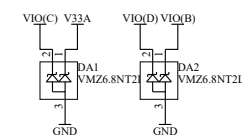
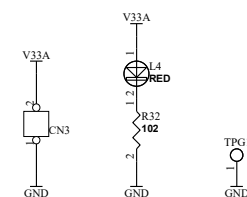
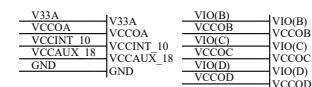
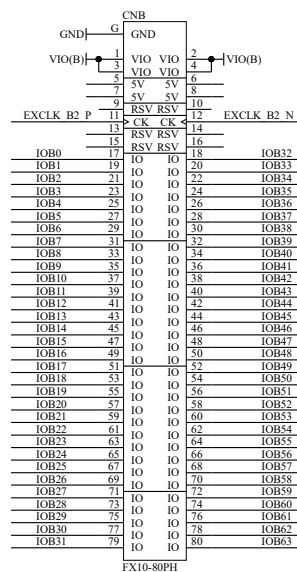
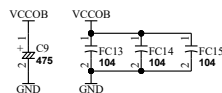




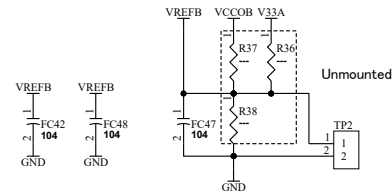
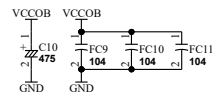


IOB[0..63]	IOB[0..63]
EXCLK B1 P	EXCLK B1 P
EXCLK B1 N	EXCLK B1 N
EXCLK B2 P	EXCLK B2 P
EXCLK B2 N	EXCLK B2 N

Pin 1 connection diagram for the 74VHC00. Pin 1 is connected to VCCOB. Pins 2, 5, 6, 3, and 7 are connected to ground.



VCCO_16
VCCO_16
VCCO_16
VCCO_16
VCCO_16
VCCO_16

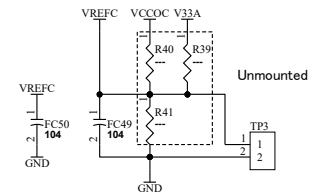
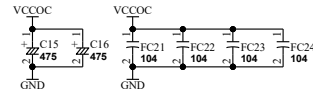


V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

IOCT0_831	
EXCLK C1 P	EXCLK C1 P
EXCLK C1 N	EXCLK C1 N
EXCLK C2 P	EXCLK C2 P
EXCLK C2 N	EXCLK C2 N

	FPGA
AB22	IO 0_12
IO13	IO L1P T0_12
IO12	IO L1N T0_12
IO67	IO L2P T0_12
IO66	IO L2N T0_12
IO15	IO L3P T0 DQS_12
IO14	IO L3N T0 DQS_12
IO11	IO L4P T0_12
IO10	IO L4N T0_12
IO16	IO L5P T0_12
IO17	IO L5N T0_12
AD23	IO L6P T0_12
AD24	IO L6N T0 VREF_12
VREFC	IO L7P T1_12
IO53	IO L7N T1_12
IO21	IO L8P T1_12
IO20	IO L8N T1_12
IO18	IO L9P T1 DQS_12
IO19	IO L9N T1 DQS_12
IO54	IO L10P T1_12
IO55	IO L10N T1_12
AB21	IO L11P T1 SRCC_12
AC21	IO L11N T1 SRCC_12
AA20	IO L12P T1 MRCC_12
AB20	IO L12N T1 MRCC_12
IO36	IO L13P T2 MRCC_12
IO37	IO L13N T2 MRCC_12
IO36	IO L14P T2 SRCC_12
IO35	IO L14N T2 SRCC_12
IO57	IO L15P T2 DQS_12
IO58	IO L15N T2 DQS_12
IO59	IO L16P T2_12
IO22	IO L16N T2_12
IO23	IO L17P T2_12
IO38	IO L17N T2_12
IO39	IO L18P T2_12
IO24	IO L18N T2_12
IO25	IO L19P T3_12
AA17	IO L19N T3 VREF_12
AB17	IO L20P T3_12
IO60	IO L20N T3_12
IO41	IO L21P T3 DQS_12
IO40	IO L21N T3 DQS_12
IO62	IO L22P T3_12
IO63	IO L22N T3_12
IO70	IO L23P T3_12
IO71	IO L23N T3_12
IO73	IO L24P T3_12
IO72	IO L24N T3_12
IO80	IO 25_12

	FPGA
IO83	U24
IO1	U25
IO0	U26
IO2	V26
IO3	W26
IO8	AB26
IO9	AC26
IO4	W25
IO5	Y26
IO6	Y25
IO7	AA25
	V24
VREFC	W24
IO30	AA24
IO31	AB25
IO45	AA22
IO44	AA23
IO47	AB24
IO46	AC24
IO26	V23
IO27	W23
IO28	Y22
IO29	Y23
EXCLK C1 P	U22
EXCLK C1 N	V22
EXCLK C2 P	U21
EXCLK C2 N	V21
IO32	W21
IO33	Y21
IO51	T20
IO50	U20
IO34	W20
IO35	Y20
IO64	T19
IO65	U19
IO42	V19
IO43	W19
IO31	V18
IO7	W18
VREFC	T14
IO76	T15
IO49	T17
IO48	T18
IO79	U15
IO78	U16
IO75	U14
IO74	V14
IO69	V16
IO68	V17
IO82	U17



HUMANDATA
 HuMANDATA LTD.
www.hdl.co.jp/ (Japan)
www2.hdl.co.jp/en/ (Global)

DSN:	TITLE: ARTIX-7 FBG676 FPGA Board Rev3
DOC. No:	XCM-208
FILE: IOC.SchDoc	DATE: 2023/09/13 11:00:47
Sheet: 4 / 7	B

