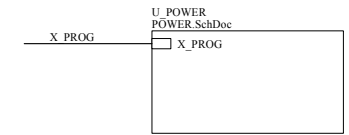
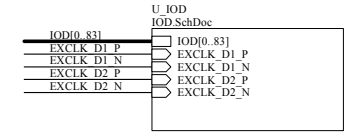
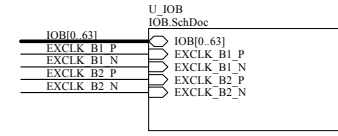
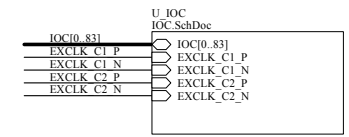
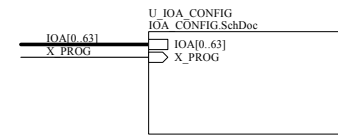
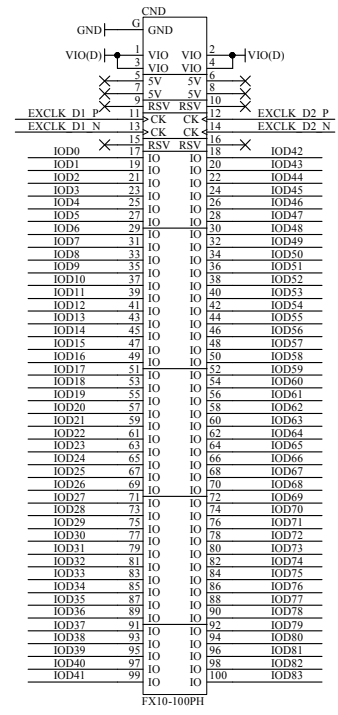
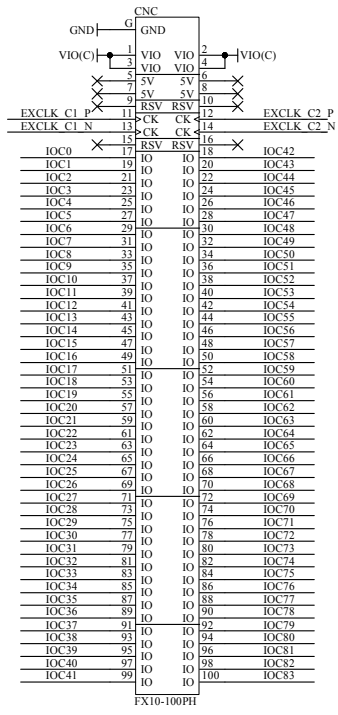
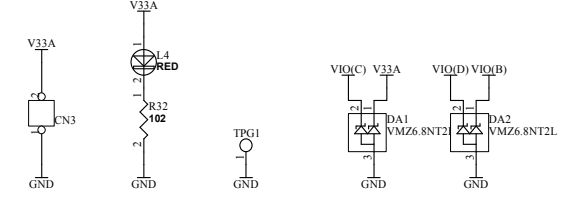


[FAN-POW] [POWER]

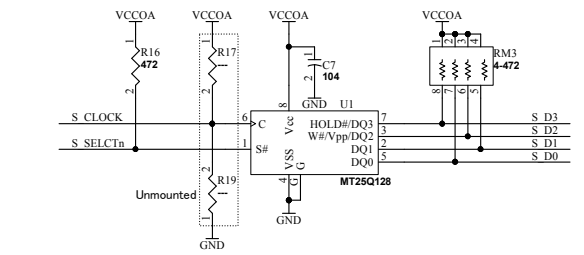
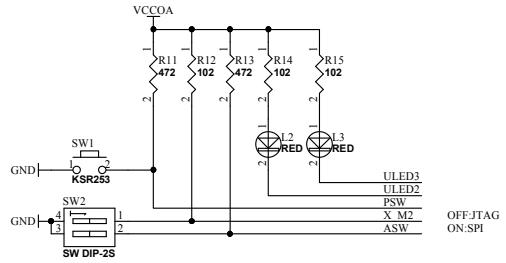
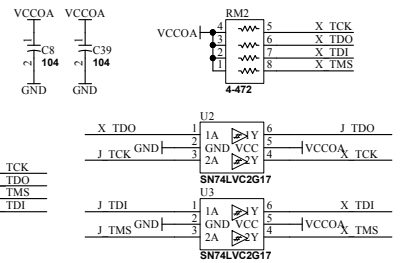
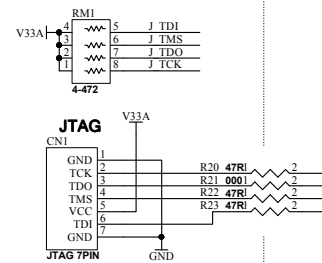
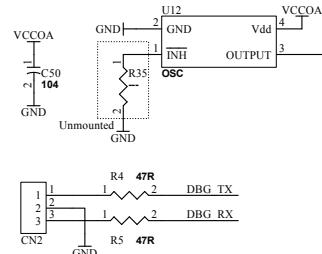
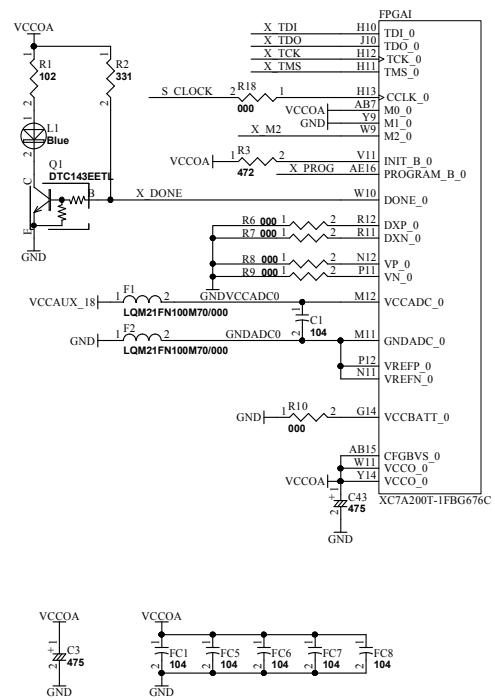
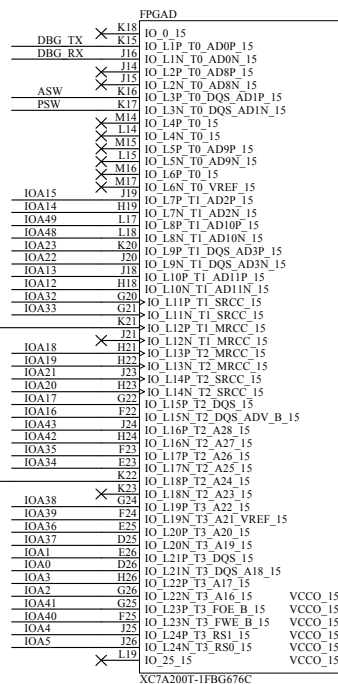
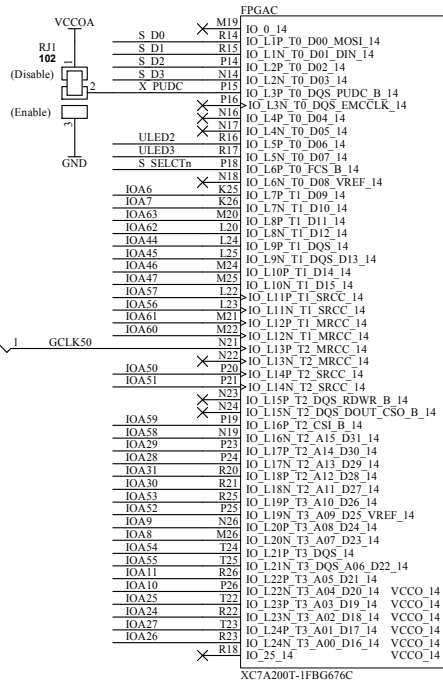
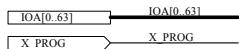


XCM208R2-SCH-A1.pdf



DSN:	TITLE: ARTIX-7 FBG676 FPGA Board Rev2	
DOC. No:	<b>XCM-208</b>	<b>A1</b>
FILE: XCM208.SchDoc	DATE: 2018/08/17 16:29:53	Sheet: 1 / 7

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

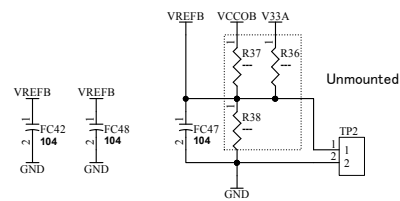
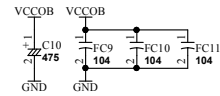
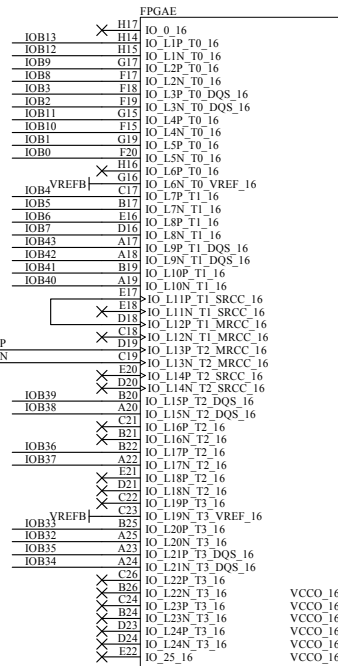
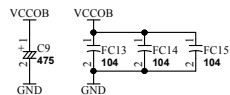
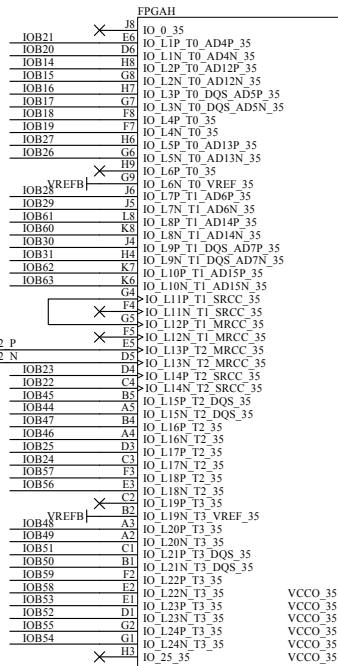
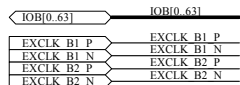


XC2M082-SCH-A1.pdf



DSN:	TITLE: ARTIX-7 FBG676 FPGA Board Rev2
DOC No:	<b>XCM-208</b>
FILE: IOA_CONFIG.SchDoc	DATE: 2018/08/17 16:29:54
Sheet: 2 / 7	

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD



XCM208R2-SCH-A1.pdf



DSN:	TITLE: ARTIX-7 FBG676 FPGA Board Rev2	
DOC. No:	<b>XCM-208</b>	<b>A1</b>
FILE: IOB.SchDoc	DATE: 2018/08/17 16:29:54	Sheet: 3 / 7

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

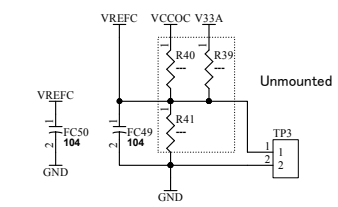
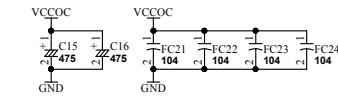
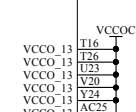
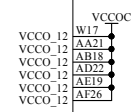
IOCI0_83I	IOCI0_83I
EXCLK C1 P	EXCLK C1 P
EXCLK C1 N	EXCLK C1 N
EXCLK C2 P	EXCLK C2 P
EXCLK C2 N	EXCLK C2 N

FPGA

IOCI13	AB22	IO_0_12
IOCI12	AE25	IO_L1P_T0_12
IOCI67	AE26	IO_L1N_T0_12
IOCI66	AC23	IO_L2P_T0_12
IOCI15	AF24	IO_L2N_T0_12
IOCI14	AF24	IO_L3P_T0_DQS_12
IOCI11	AD25	IO_L3N_T0_DQS_12
IOCI10	AD26	IO_L4P_T0_12
IOCI16	AE23	IO_L4N_T0_12
IOCI17	AF23	IO_L5P_T0_12
	AD23	IO_L5N_T0_12
	AD24	IO_L6P_T0_12
IOCS2	AD21	IO_L6N_T0_VREF_12
IOCS3	AE21	IO_L7P_T1_12
IOCI21	AF19	IO_L7N_T1_12
IOCI20	AF20	IO_L8P_T1_12
IOCI18	AE22	IO_L8N_T1_12
IOCI19	AF22	IO_L9P_T1_DQS_12
IOCS4	AD20	IO_L9N_T1_DQS_12
IOCS5	AE20	IO_L10P_T1_12
	AE20	IO_L10N_T1_12
	AB21	IO_L11P_T1_SRCC_12
	AC21	IO_L11N_T1_SRCC_12
	AA20	IO_L12P_T1_MRCC_12
	AB20	IO_L12N_T1_MRCC_12
IOCS6	AA19	IO_L13P_T2_MRCC_12
IOCS7	AB19	IO_L13N_T2_MRCC_12
IOCS6	AC19	IO_L14P_T2_SRCC_12
IOCS5	AD19	IO_L14N_T2_SRCC_12
IOCS8	AC18	IO_L15P_T2_DQS_12
IOCS9	AD18	IO_L15N_T2_DQS_12
IOCI22	AE18	IO_L16P_T2_12
IOCI23	AF18	IO_L16N_T2_12
IOCI38	Y18	IO_L17P_T2_12
IOCI39	AA18	IO_L17N_T2_12
IOCI24	AE17	IO_L18P_T2_12
IOCI25	AF17	IO_L18N_T2_12
	AA17	IO_L19P_T3_12
	AB17	IO_L19N_T3_VREF_12
IOCI6	AC17	IO_L20P_T3_12
IOCI60	AD17	IO_L20N_T3_12
IOCI41	Y16	IO_L21P_T3_DQS_12
IOCI40	Y17	IO_L21N_T3_DQS_12
IOCI62	AB16	IO_L22P_T3_12
IOCI63	AC16	IO_L22N_T3_12
IOCI70	Y15	IO_L23P_T3_12
IOCI71	AA15	IO_L23N_T3_12
IOCI73	W14	IO_L24P_T3_12
IOCI72	W15	IO_L24N_T3_12
IOCI80	W16	IO_25_12

FPGA

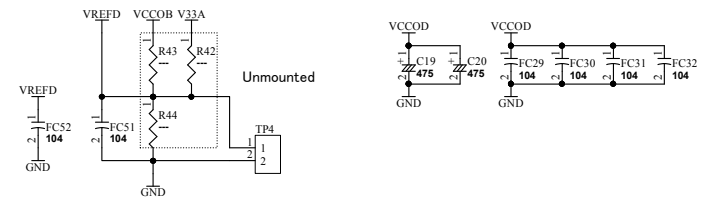
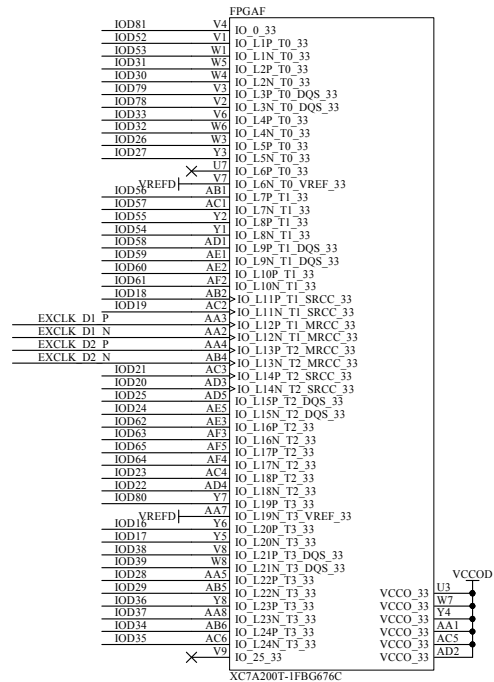
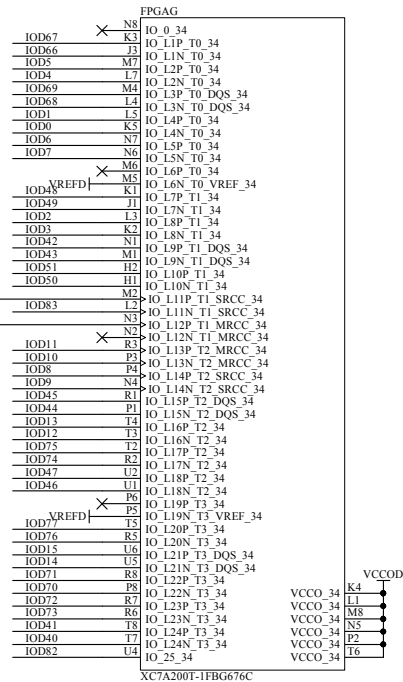
IOCI83	U24	IO_0_13
IOCI1	U25	IO_L1P_T0_13
IOCI0	U26	IO_L1N_T0_13
IOCI2	V26	IO_L2P_T0_13
IOCI3	W26	IO_L2N_T0_13
IOCI8	AB26	IO_L3P_T0_DQS_13
IOCI9	AC26	IO_L3N_T0_DQS_13
IOCI4	AD26	IO_L4P_T0_13
IOCI5	Y26	IO_L4N_T0_13
IOCI6	Y25	IO_L5P_T0_13
IOCI7	AA25	IO_L5N_T0_13
	V24	IO_L6P_T0_13
	W24	IO_L6N_T0_VREF_13
IOCI30	AA24	IO_L7P_T1_13
IOCI31	AB25	IO_L7N_T1_13
IOCI45	AA22	IO_L8P_T1_13
IOCI44	AA23	IO_L8N_T1_13
IOCI47	AB24	IO_L9P_T1_DQS_13
IOCI46	AC24	IO_L9N_T1_DQS_13
IOCI26	V23	IO_L10P_T1_13
IOCI27	W23	IO_L10N_T1_13
IOCI28	Y23	IO_L11P_T1_SRCC_13
IOCI29	Y23	IO_L11N_T1_SRCC_13
	U22	IO_L12P_T1_MRCC_13
	V22	IO_L12N_T1_MRCC_13
	U21	IO_L13P_T2_MRCC_13
	U21	IO_L13N_T2_MRCC_13
	W21	IO_L14P_T2_SRCC_13
IOCI32	W21	IO_L14N_T2_SRCC_13
IOCI33	Y21	IO_L15P_T2_DQS_13
IOCI51	T20	IO_L15N_T2_DQS_13
IOCI50	U20	IO_L16P_T2_13
IOCI4	W20	IO_L16N_T2_13
IOCI35	Y20	IO_L17P_T2_13
IOCI64	T19	IO_L17N_T2_13
IOCI65	U19	IO_L18P_T2_13
IOCI42	V19	IO_L18N_T2_13
IOCI43	W19	IO_L19P_T3_13
IOCI81	Y18	IO_L19N_T3_VREF_13
	W18	IO_L20P_T3_13
IOCI	T14	IO_L20N_T3_13
IOCI76	T15	IO_L21P_T3_DQS_13
IOCI49	T17	IO_L21N_T3_DQS_13
IOCI48	T18	IO_L22P_T3_13
IOCI79	U15	IO_L22N_T3_13
IOCI78	U16	IO_L23P_T3_13
IOCI75	U14	IO_L23N_T3_13
IOCI74	V14	IO_L24P_T3_13
IOCI69	V16	IO_L24N_T3_13
IOCI68	V17	IO_25_13
IOCI82	U17	



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DOC. No:	<b>XCM-208</b>
FILE: IOC.SchDoc	DATE: 2018/08/17 16:29:54
Sheet: 4 / 7	<b>A1</b>

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

IOD[0..83]		IOD[0..83]	
EXCLK D1 P	EXCLK D1 P	EXCLK D1 N	EXCLK D1 N
EXCLK D2 P	EXCLK D2 P	EXCLK D2 N	EXCLK D2 N



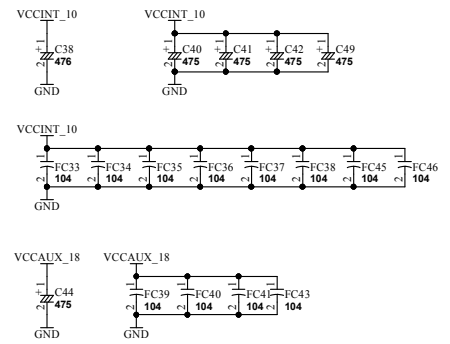
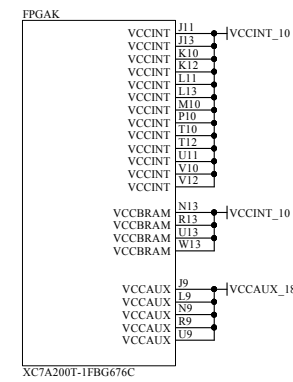
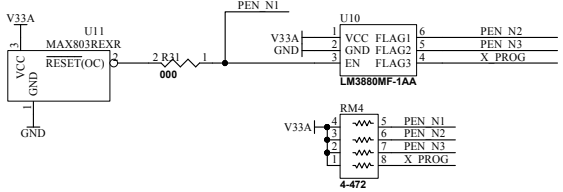
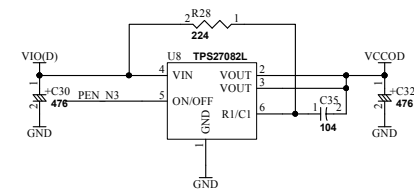
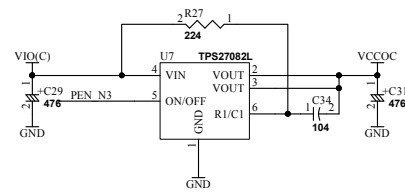
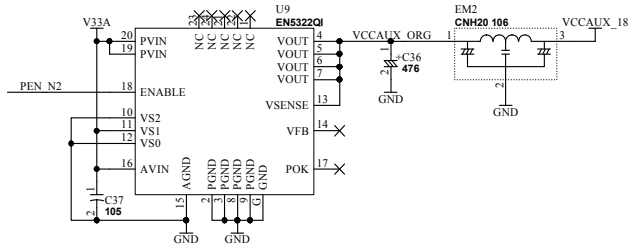
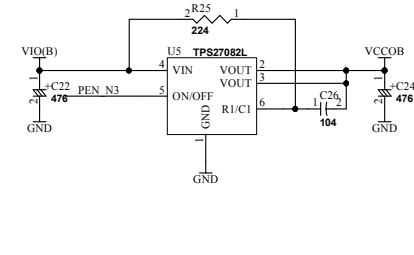
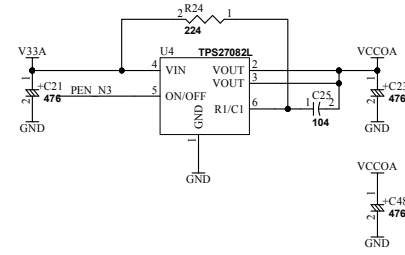
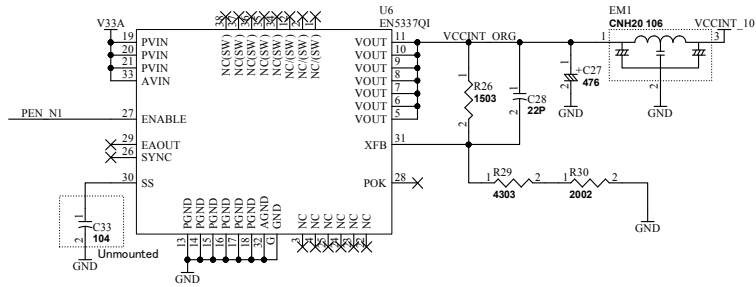
XCM208R2-SCH-A1.pdf



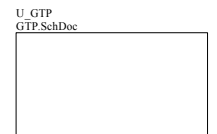
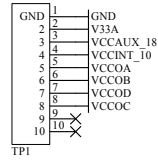
DSN:	TITLE: ARTIX-7 FBG676 FPGA Board Rev2
DOC. No: XCM-208	A1
FILE: IOD.SchDoc	DATE: 2018/08/17 16:29:54
Sheet: 5 / 7	V5.20150107

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

X\_PROG X\_PROG



Power sense point

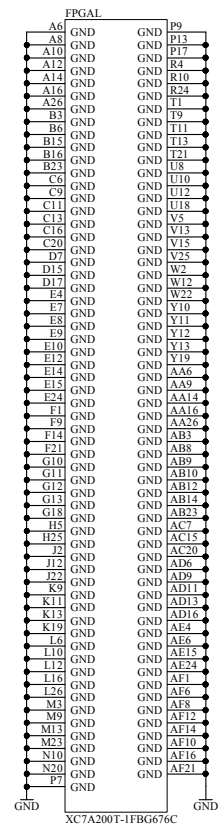
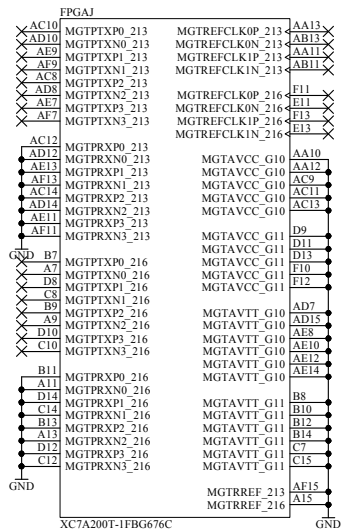


XCM2082-SCH-A1.pdf



DSN:	TITLE: ARTIX-7 FBG676 FPGA Board Rev2
DOC. No:	<b>XCM-208</b>
FILE: POWER.SchDoc	DATE: 2018/08/17 16:29:54
Sheet: 6 / 7	<b>A1</b>

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD



DSN:	TITLE: ARTIX-7 FBG676 FPGA Board Rev2	<b>A1</b>
DOC. No:	<b>XCM-208</b>	
FILE: GTP.SchDoc	DATE: 2018/08/17 16:29:54	Sheet: 7 / 7