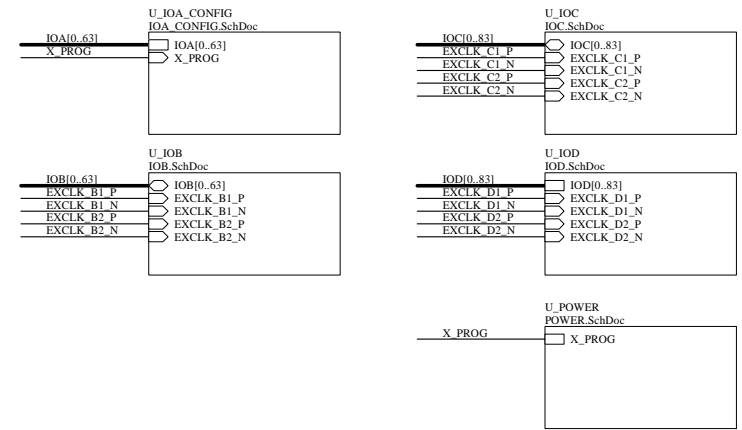
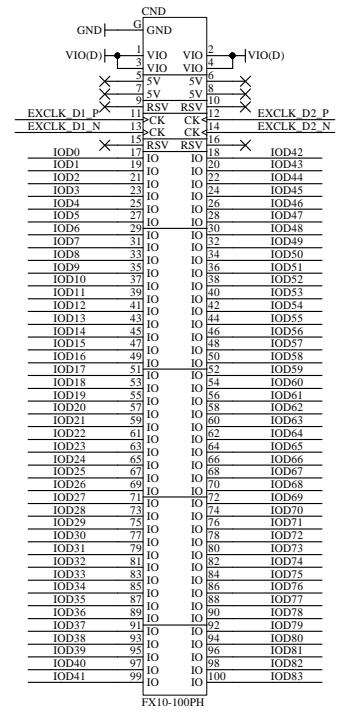
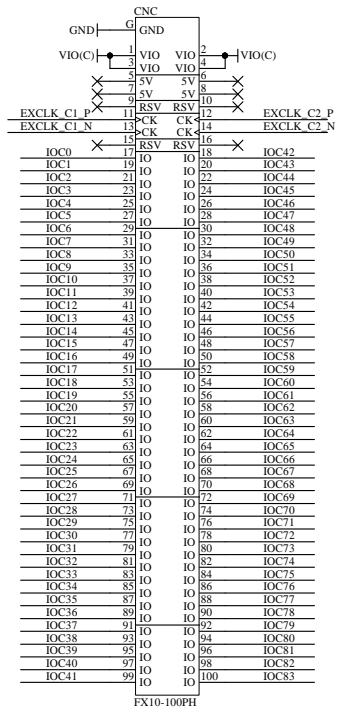
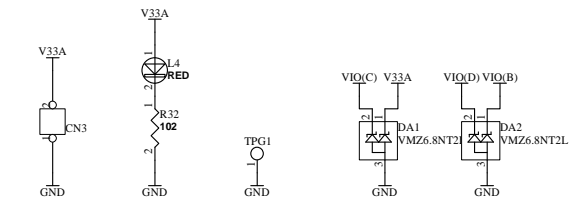


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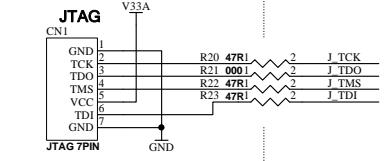
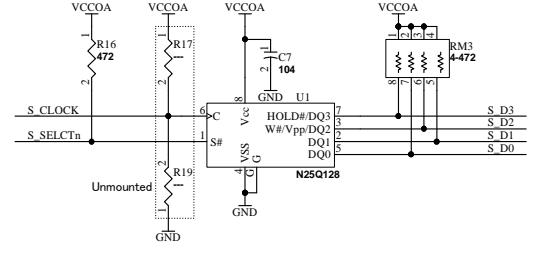
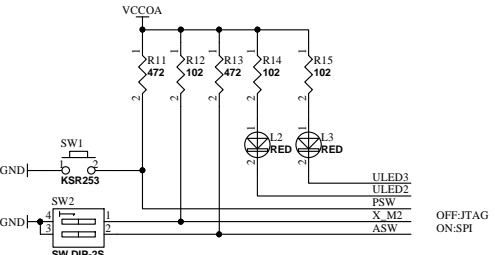
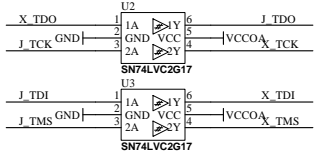
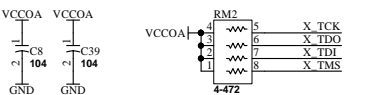
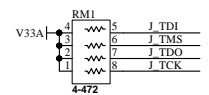
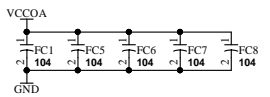
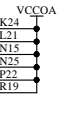
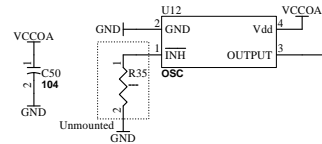
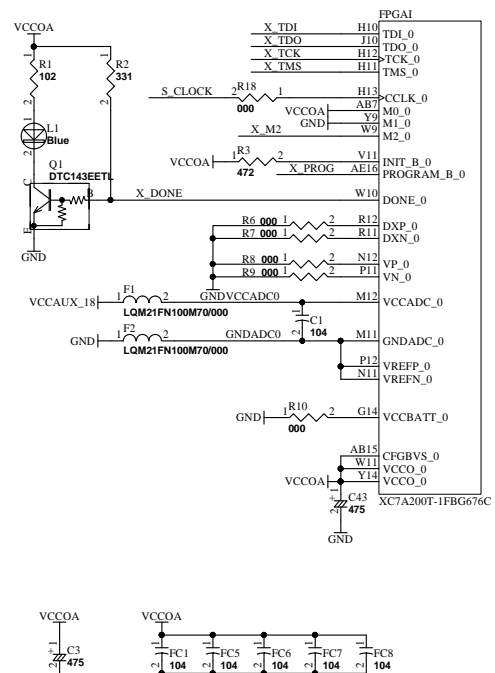
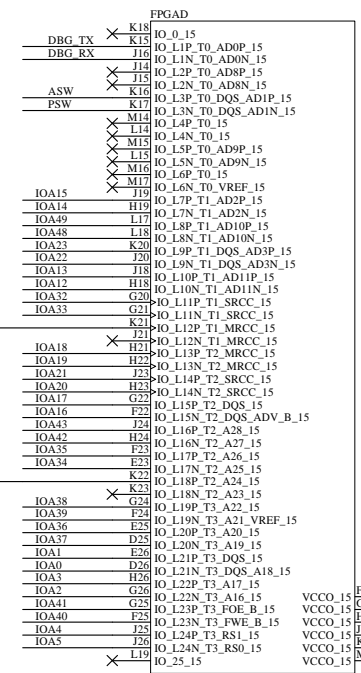
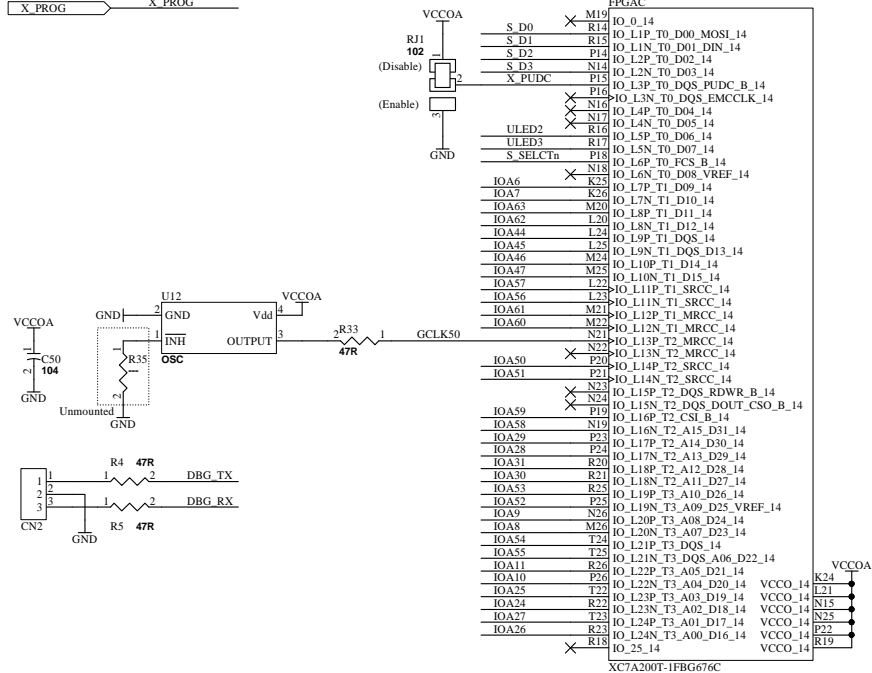
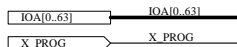


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DOC. No:	XCM-208	A
FILE: XCM208.SchDoc	DATE: 2015/10/30 11:45:56	Sheet: 1 / 7

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

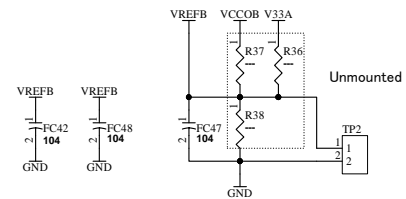
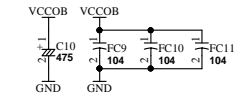
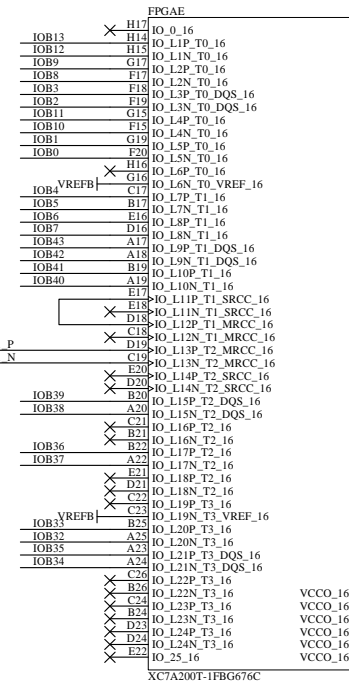
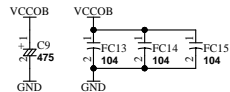
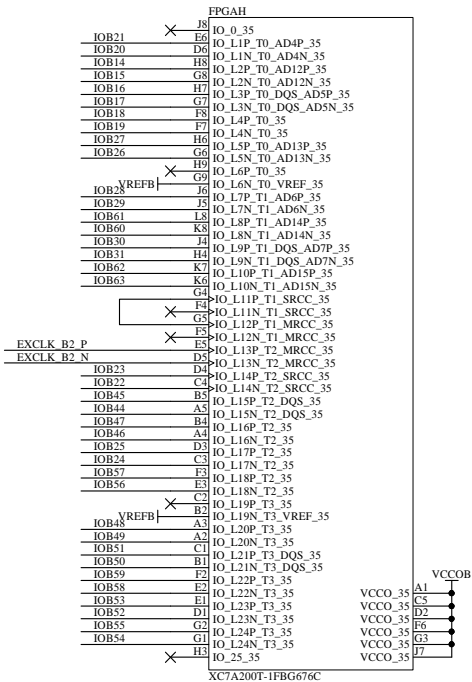
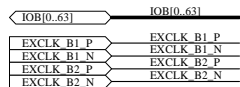


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DOC. No:	XCM-208
FILE: IOA.CONFIG.SchDoc	DATE: 2015/10/30 11:45:56
Sheet: 2	7

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VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD



XCM0208R1-SCH-A.pdf



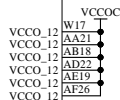
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DOC. No:	XCM-208	A
FILE: IOB.SchDoc	DATE: 2015/10/30 11:45:56	Sheet: 3 / 7

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

IOC[0..83]	IOC[0..83]
EXCLK C1 P	EXCLK C1 P
EXCLK C1 N	EXCLK C1 N
EXCLK C2 P	EXCLK C2 P
EXCLK C2 N	EXCLK C2 N

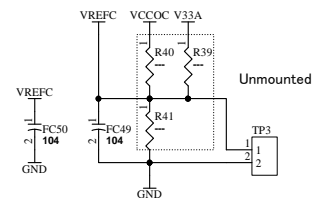
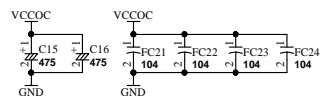
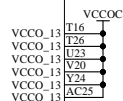
FPGA

IOC13	AB22	IO_0_12
IOC12	AE26	IO_L1P_T0_12
IOC67	AC27	IO_L1N_T0_12
IOC66	AC23	IO_L2P_T0_12
IOC15	AF24	IO_L2N_T0_12
IOC14	AF24	IO_L3P_T0_DQS_12
IOC11	AD25	IO_L3N_T0_DQS_12
IOC10	AD26	IO_L4P_T0_12
IOC16	AE23	IO_L4N_T0_12
IOC17	AF23	IO_L5P_T0_12
	AD23	IO_L5N_T0_12
	AD24	IO_L6P_T0_12
YREFC	AD21	IO_L6N_T0_VREF_12
IOC52	AE21	IO_L7P_T1_12
IOC21	AF19	IO_L7N_T1_12
IOC20	AF20	IO_L8P_T1_12
IOC18	AE22	IO_L8N_T1_12
IOC19	AF22	IO_L9P_T1_DQS_12
IOC54	AD20	IO_L9N_T1_DQS_12
IOC55	AE20	IO_L10P_T1_12
	AB21	IO_L10N_T1_12
	AC21	IO_L11P_T1_SRCC_12
	AA20	IO_L11N_T1_SRCC_12
	AB20	IO_L12P_T1_MRCC_12
IOC36	AA19	IO_L12N_T1_MRCC_12
IOC37	AB19	IO_L13P_T2_MRCC_12
IOC56	AC19	IO_L13N_T2_MRCC_12
IOC57	AD19	IO_L14P_T2_SRCC_12
IOC58	AC18	IO_L14N_T2_SRCC_12
IOC59	AD18	IO_L15P_T2_DQS_12
IOC22	AE18	IO_L15N_T2_DQS_12
IOC25	AF18	IO_L16P_T2_12
IOC38	Y18	IO_L16N_T2_12
IOC39	AA18	IO_L17P_T2_12
IOC24	AE17	IO_L17N_T2_12
IOC25	AF17	IO_L18P_T2_12
	AA17	IO_L18N_T2_12
	AB17	IO_L19P_T3_12
YREFC	AC17	IO_L19N_T3_VREF_12
IOC61	AD17	IO_L20P_T3_12
IOC41	Y16	IO_L20N_T3_12
IOC40	Y17	IO_L21P_T3_DQS_12
IOC62	AB16	IO_L21N_T3_DQS_12
IOC63	AC16	IO_L22P_T3_12
IOC70	Y15	IO_L22N_T3_12
IOC71	AA15	IO_L23P_T3_12
IOC73	W14	IO_L23N_T3_12
IOC72	W15	IO_L24P_T3_12
IOC80	W16	IO_L24N_T3_12
		IO_25_12



FPGA

IOC83	U24	IO_0_13
IOC1	U25	IO_L1P_T0_13
IOC0	U26	IO_L1N_T0_13
IOC2	V26	IO_L2P_T0_13
IOC3	W26	IO_L2N_T0_13
IOC8	AB26	IO_L3P_T0_DQS_13
IOC9	AC26	IO_L3N_T0_DQS_13
IOC4	W25	IO_L4P_T0_13
IOC5	Y26	IO_L4N_T0_13
IOC6	Y25	IO_L5P_T0_13
IOC7	AA25	IO_L5N_T0_13
	V24	IO_L6P_T0_13
	W24	IO_L6N_T0_VREF_13
YREFC	AA24	IO_L7P_T1_13
IOC30	AB25	IO_L7N_T1_13
IOC31	AB25	IO_L7N_T1_13
IOC45	AA22	IO_L8P_T1_13
IOC44	AA23	IO_L8N_T1_13
IOC47	AB24	IO_L9P_T1_DQS_13
IOC46	AC24	IO_L9N_T1_DQS_13
IOC26	V23	IO_L10P_T1_13
IOC27	W23	IO_L10N_T1_13
IOC28	Y22	IO_L11P_T1_SRCC_13
IOC29	Y23	IO_L11N_T1_SRCC_13
	U22	IO_L12P_T1_MRCC_13
EXCLK C1 P	V22	IO_L12N_T1_MRCC_13
EXCLK C1 N	U21	IO_L13P_T2_MRCC_13
EXCLK C2 P	U21	IO_L13N_T2_MRCC_13
EXCLK C2 N	W21	IO_L14P_T2_SRCC_13
	Y21	IO_L14N_T2_SRCC_13
IOC32	W21	IO_L15P_T2_DQS_13
IOC33	Y21	IO_L15N_T2_DQS_13
IOC51	T20	IO_L16P_T2_13
IOC50	U20	IO_L16N_T2_13
IOC34	W20	IO_L17P_T2_13
IOC35	Y20	IO_L17N_T2_13
IOC64	T19	IO_L18P_T2_13
IOC65	U19	IO_L18N_T2_13
IOC42	V19	IO_L19P_T3_13
IOC43	W19	IO_L19N_T3_VREF_13
IOC81	V18	IO_L20P_T3_13
	W18	IO_L20N_T3_13
YREFC	T14	IO_L21P_T3_DQS_13
IOC76	T15	IO_L21N_T3_DQS_13
IOC49	T17	IO_L22P_T3_13
IOC48	T18	IO_L22N_T3_13
IOC79	U15	IO_L23P_T3_13
IOC78	U16	IO_L23N_T3_13
IOC75	U14	IO_L24P_T3_13
IOC74	V14	IO_L24N_T3_13
IOC69	V16	IO_25_13
IOC68	V17	
IOC82	U17	



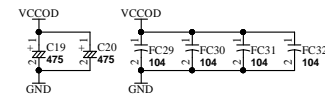
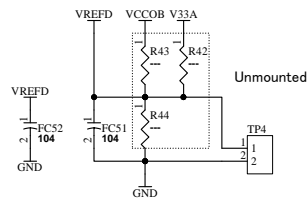
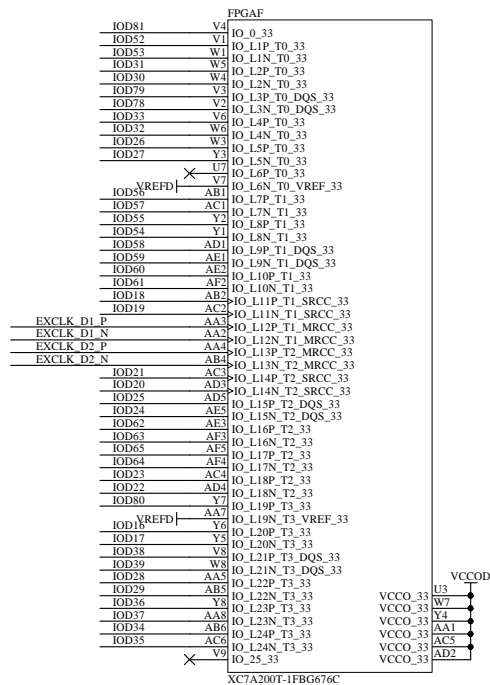
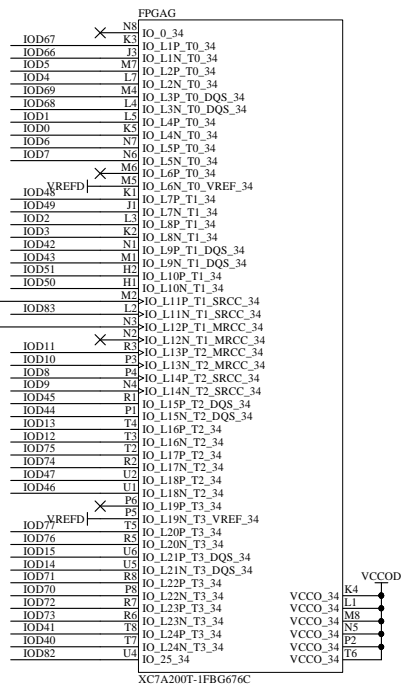
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DOC. No:	XCM-208	A
FILE: IOC.SchDoc	DATE: 2015/10/30 11:45:56	Sheet: 4 / 7

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

IOD[0..83]	IOD[0..83]
EXCLK D1 P	EXCLK D1 P
EXCLK D1 N	EXCLK D1 N
EXCLK D2 P	EXCLK D2 P
EXCLK D2 N	EXCLK D2 N



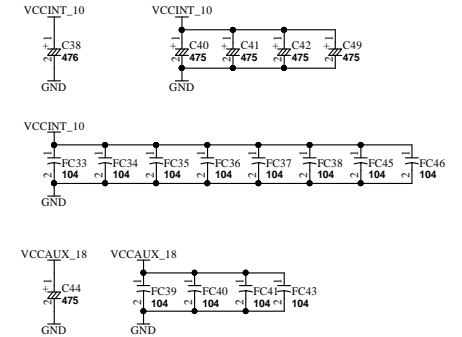
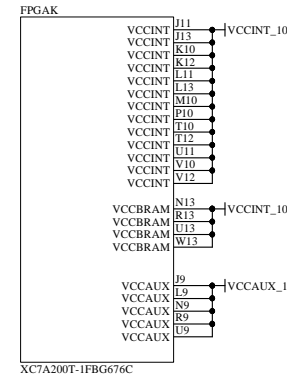
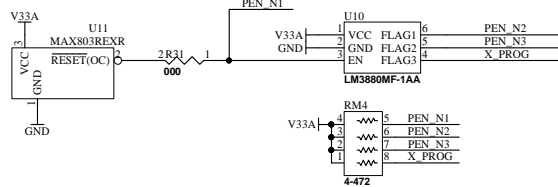
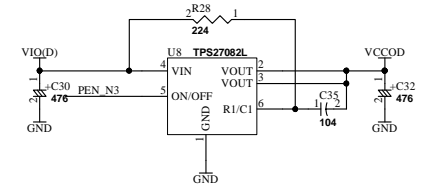
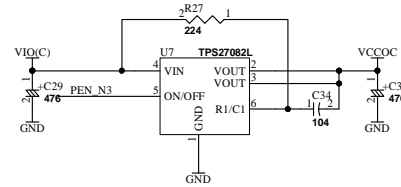
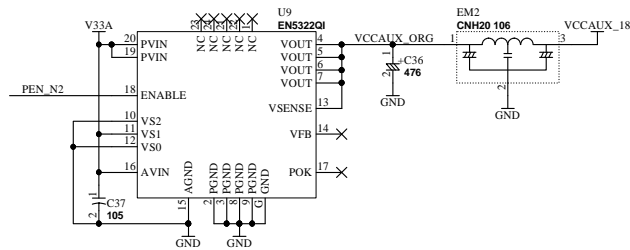
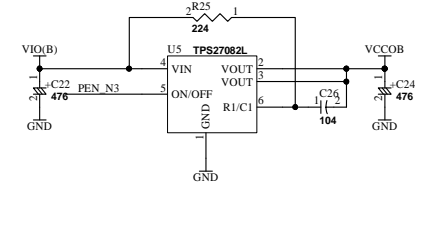
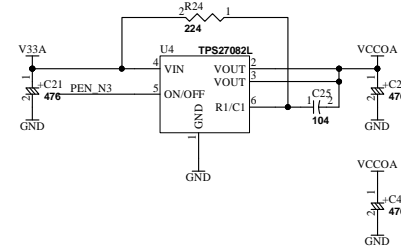
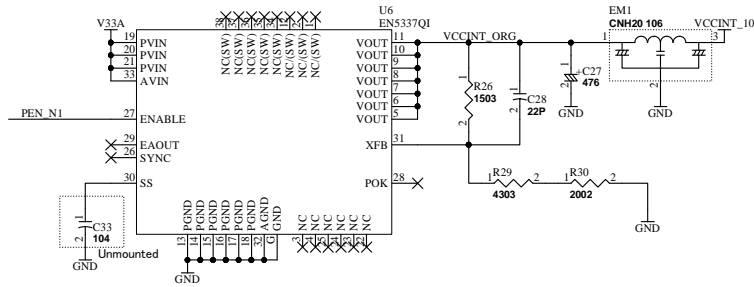
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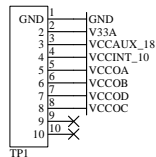
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DOC. No: XCM-208	A
FILE: IOD.SchDoc	DATE: 2015/10/30 11:45:56
Sheet: 5 / 7	V5.20150107

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD

X_PROG X_PROG



Power sense point



U_GTP
GTP.SchDoc

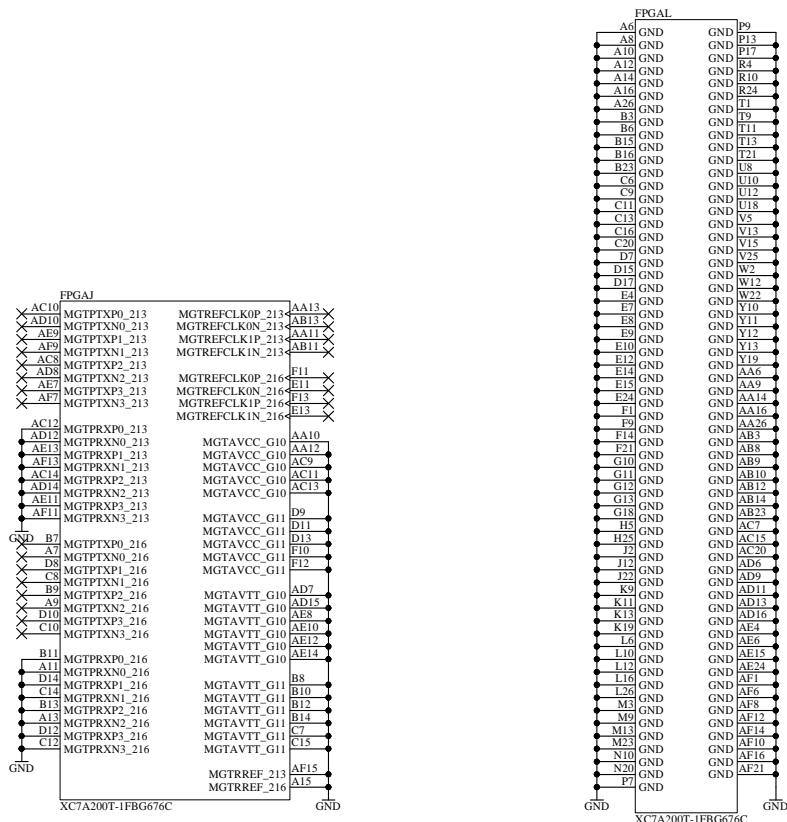


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DSN:	TITLE: ARTIX-7 FBG676 FPGA Board
DOC. No:	XCM-208
FILE: POWER.SchDoc	DATE: 2015/10/30 11:45:56
Sheet: 6	7

V33A	V33A	VIO(B)	VIO(B)
VCCOA	VCCOA	VCCOB	VCCOB
VCCINT_10	VCCINT_10	VIO(C)	VIO(C)
VCCAUX_18	VCCAUX_18	VCCOC	VCCOC
GND	GND	VIO(D)	VIO(D)
		VCCOD	VCCOD



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DOC. No:	XCM-208
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