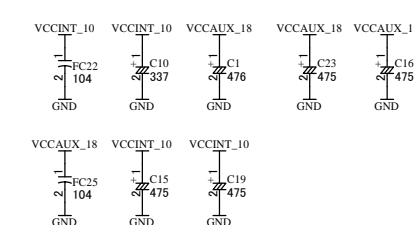
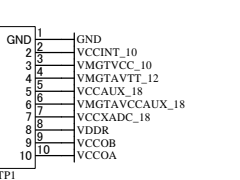
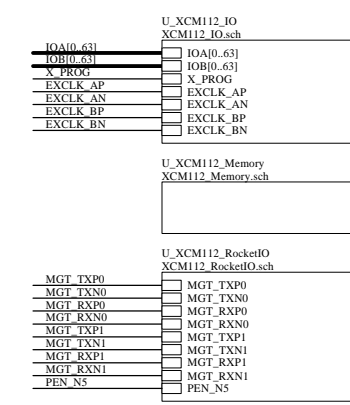
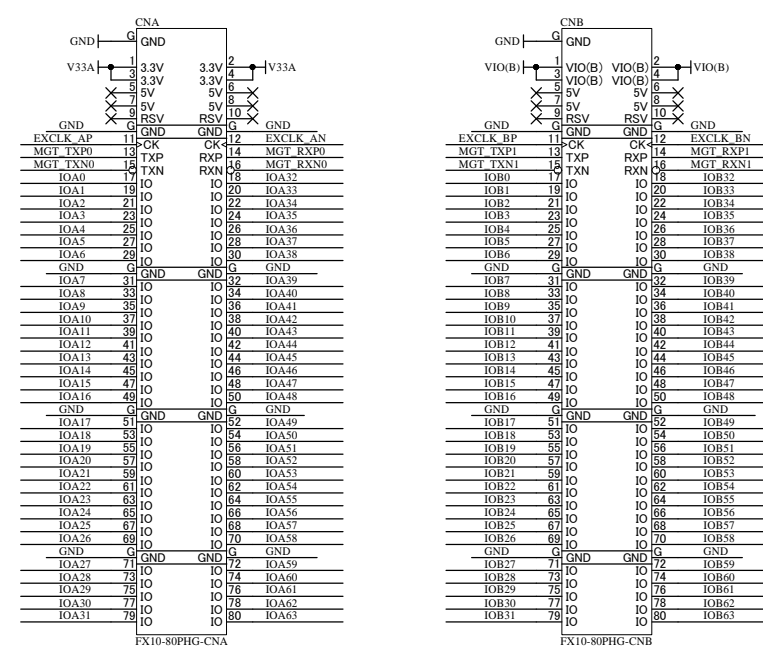
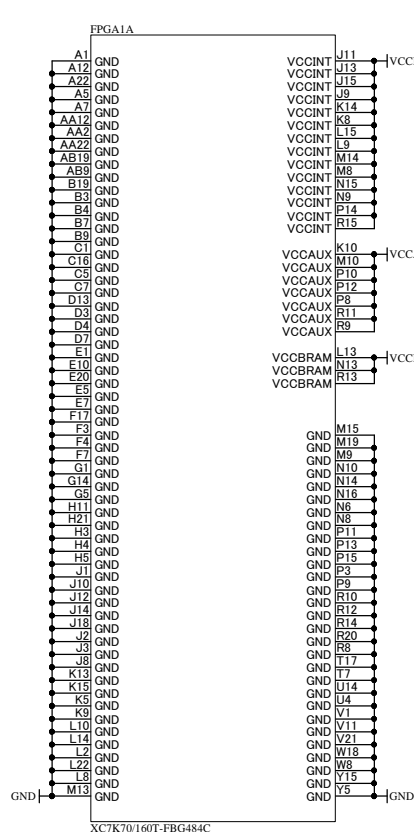
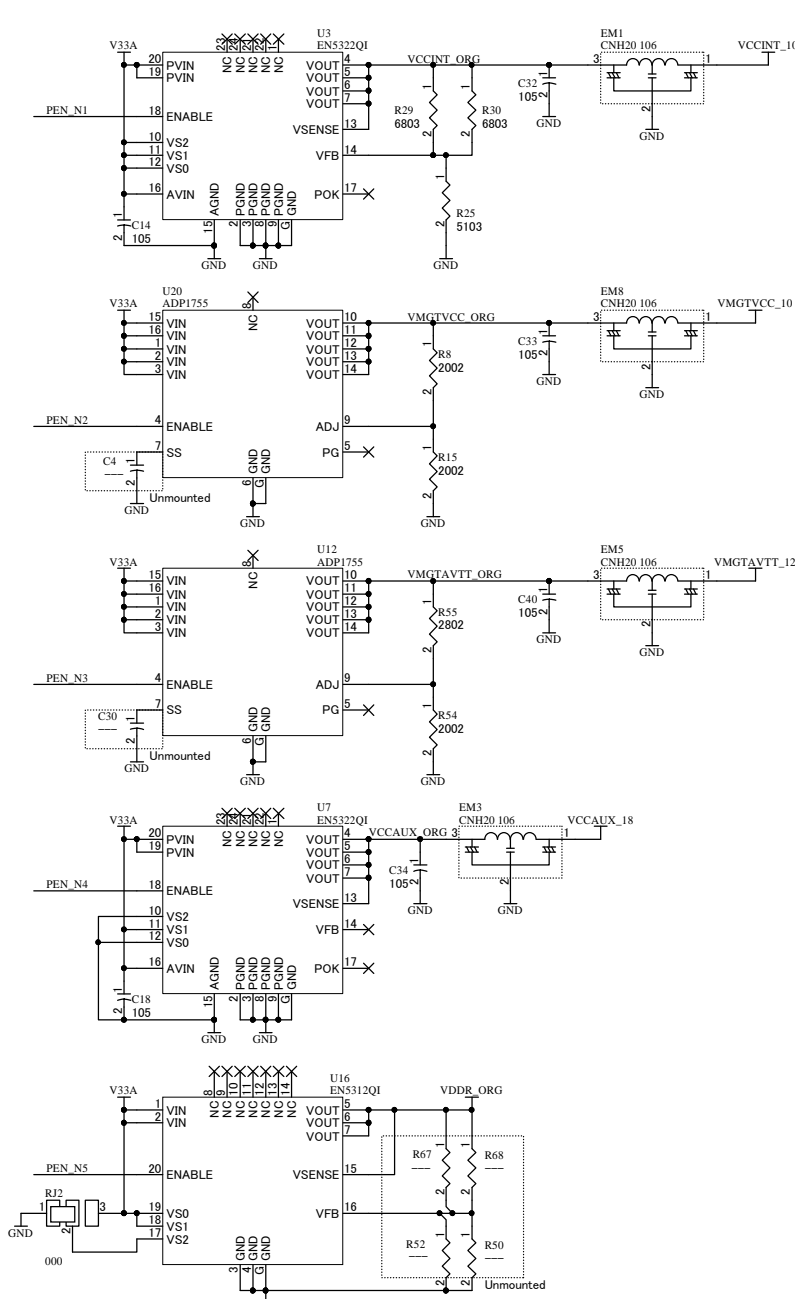
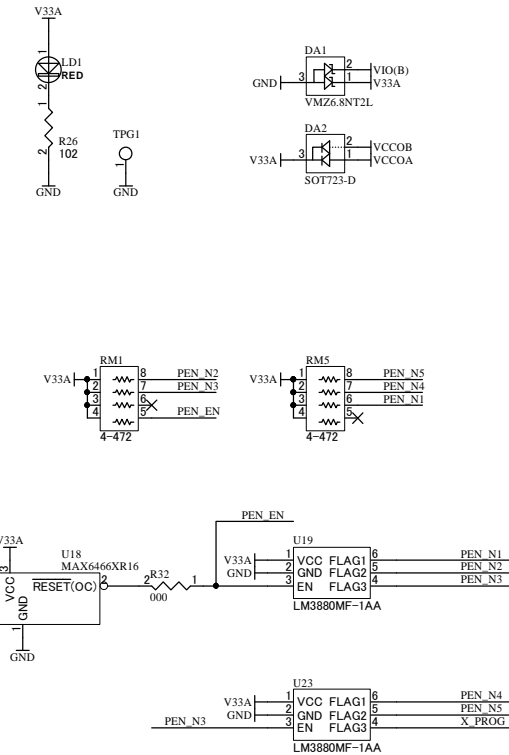


V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVCC_10	VMGTAVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VDDR_ORG	VDDR_ORG
VCCOA	VCCOA
VCCOB	VCCOB
VMGTAVCCAUX_18	VMGTAVCCAUX_18
VCCXADC_18	VCCXADC_18
GND	GND

[POWER]



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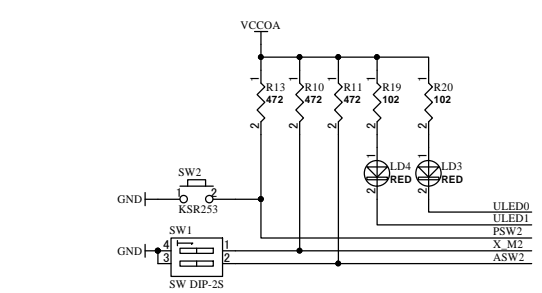
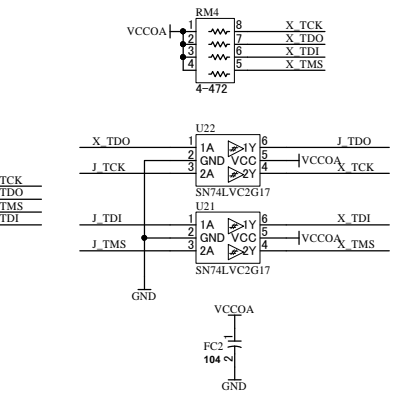
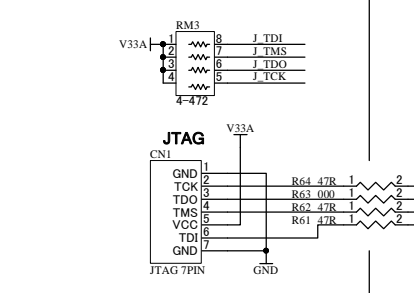
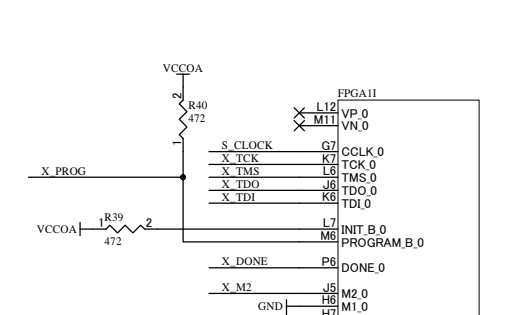
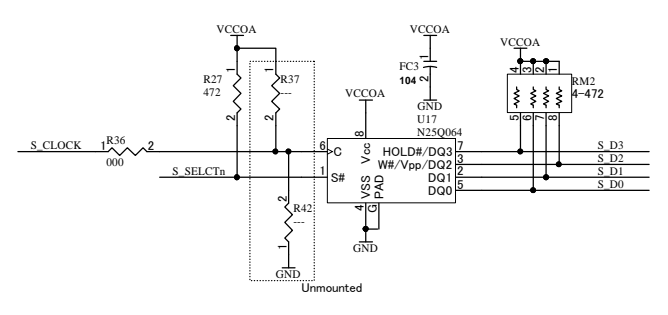
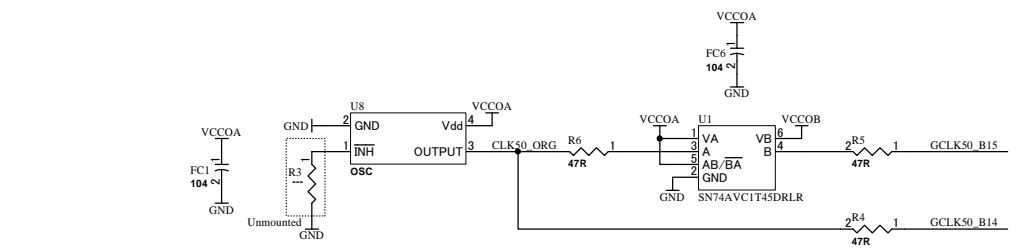
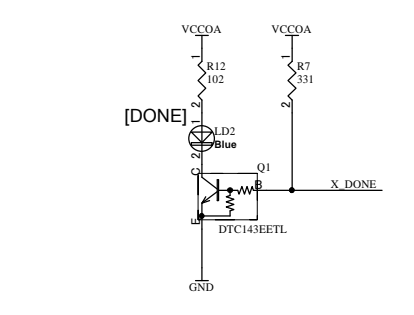
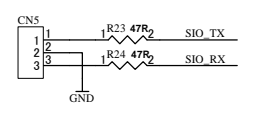
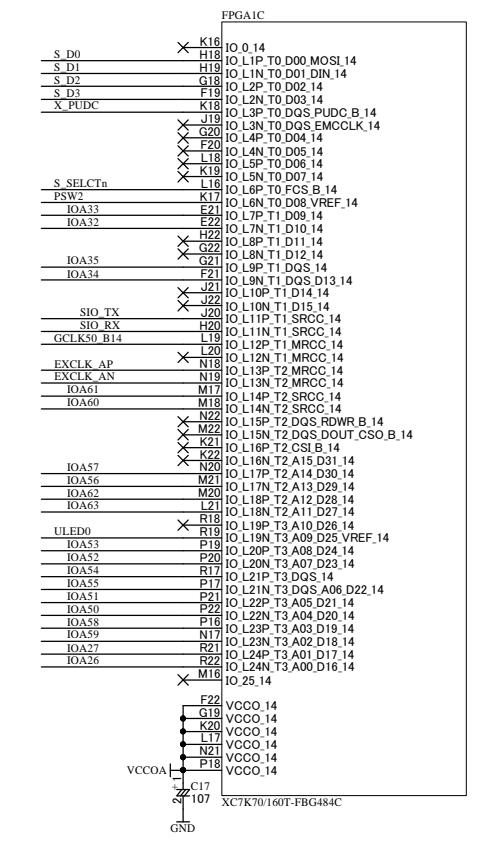
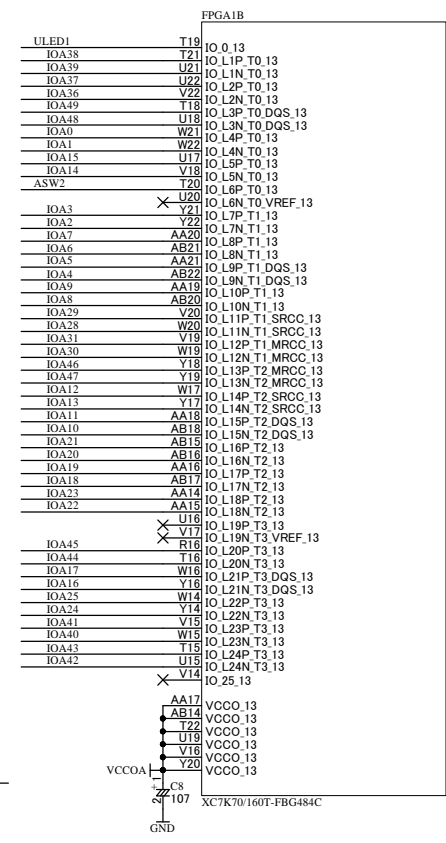
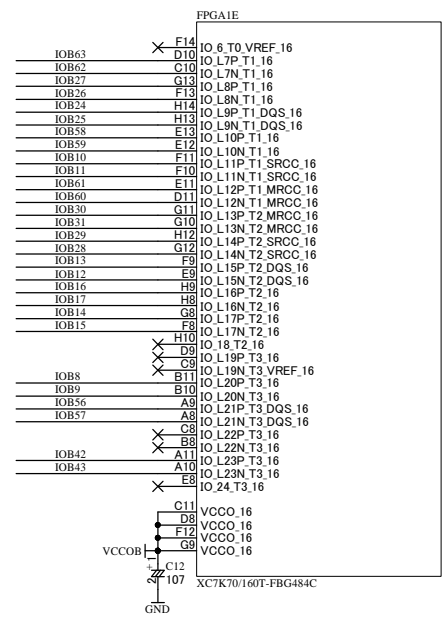
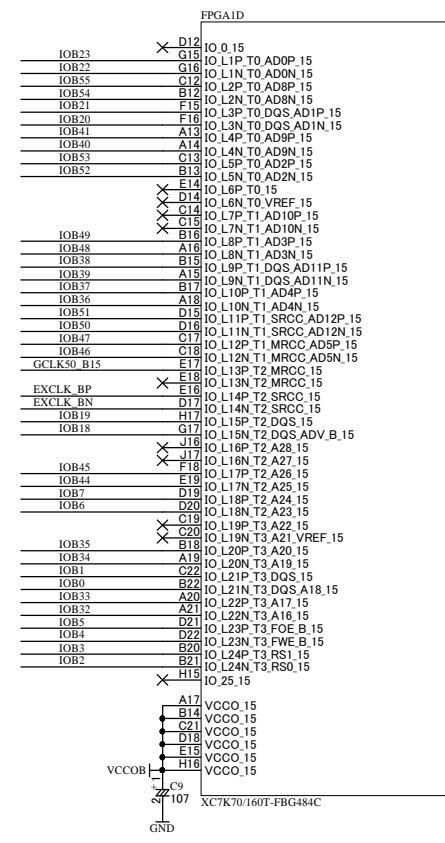
KINTEX FBG484 FPGA Board

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			DOC. No.	XCM-112	B			

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VDDR_ORG	VDDR_ORG
VCCOA	VCCOA
VCCOB	VCCOB
VMGTAVCCAUX_18	VMGTAVCCAUX_18
VCCXADC_18	VCCXADC_18
GND	GND

BANK Group B **BANK Group A**

IOA[0..63]	IOA[0..63]
IOB[0..63]	IOB[0..63]
EXCLK AP	EXCLK AP
EXCLK AN	EXCLK AN
EXCLK BP	EXCLK BP
EXCLK BN	EXCLK BN
X PROG	X PROG

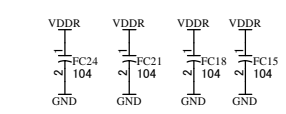
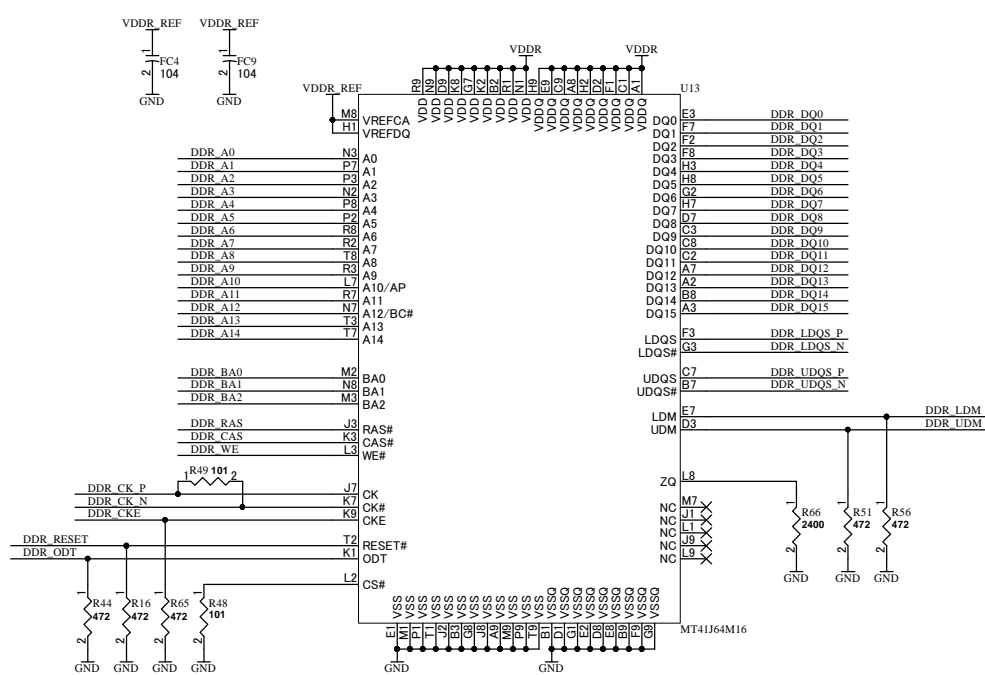
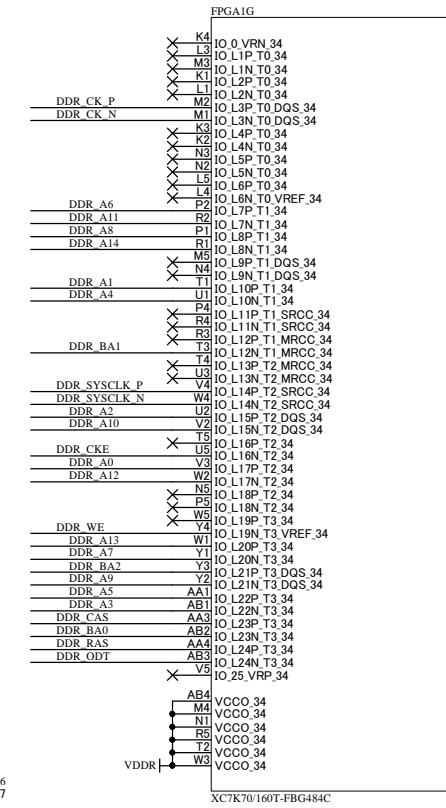
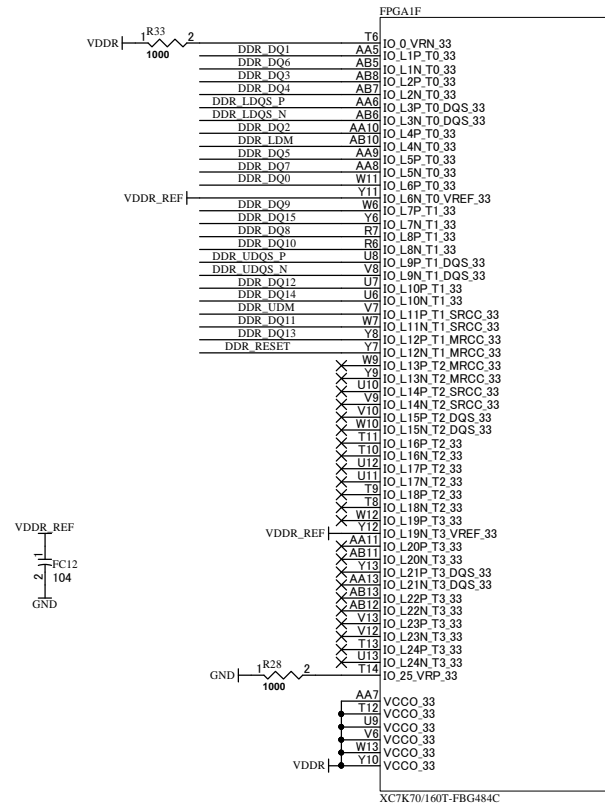
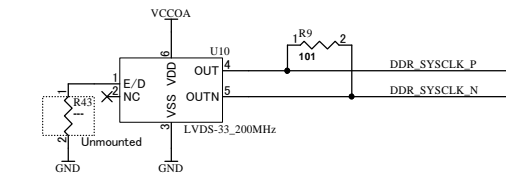
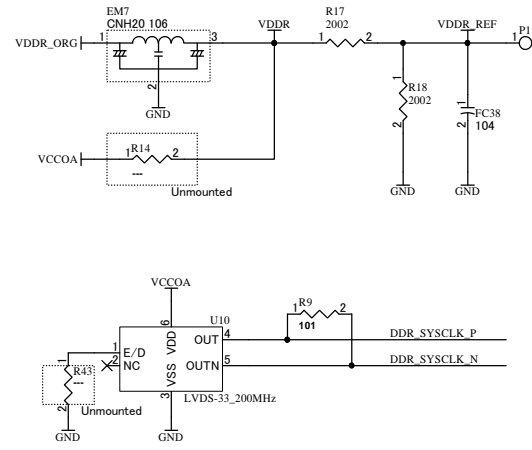


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DOC. No.	XCM-112	B
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V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVTT_10	VMGTAVTT_10
VCCAVTT_12	VCCAVTT_12
VCCAUX_18	VCCAUX_18
VDDR_ORG	VDDR_ORG
VCCOA	VCCOA
VCCOB	VCCOB
VMGTAVCCAUX_18	VMGTAVCCAUX_18
VCCXADC_18	VCCXADC_18
GND	GND



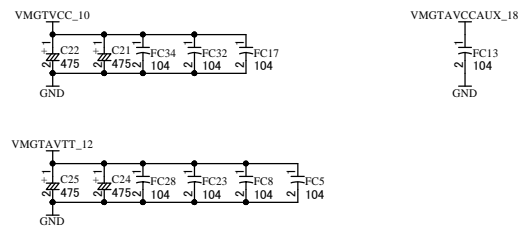
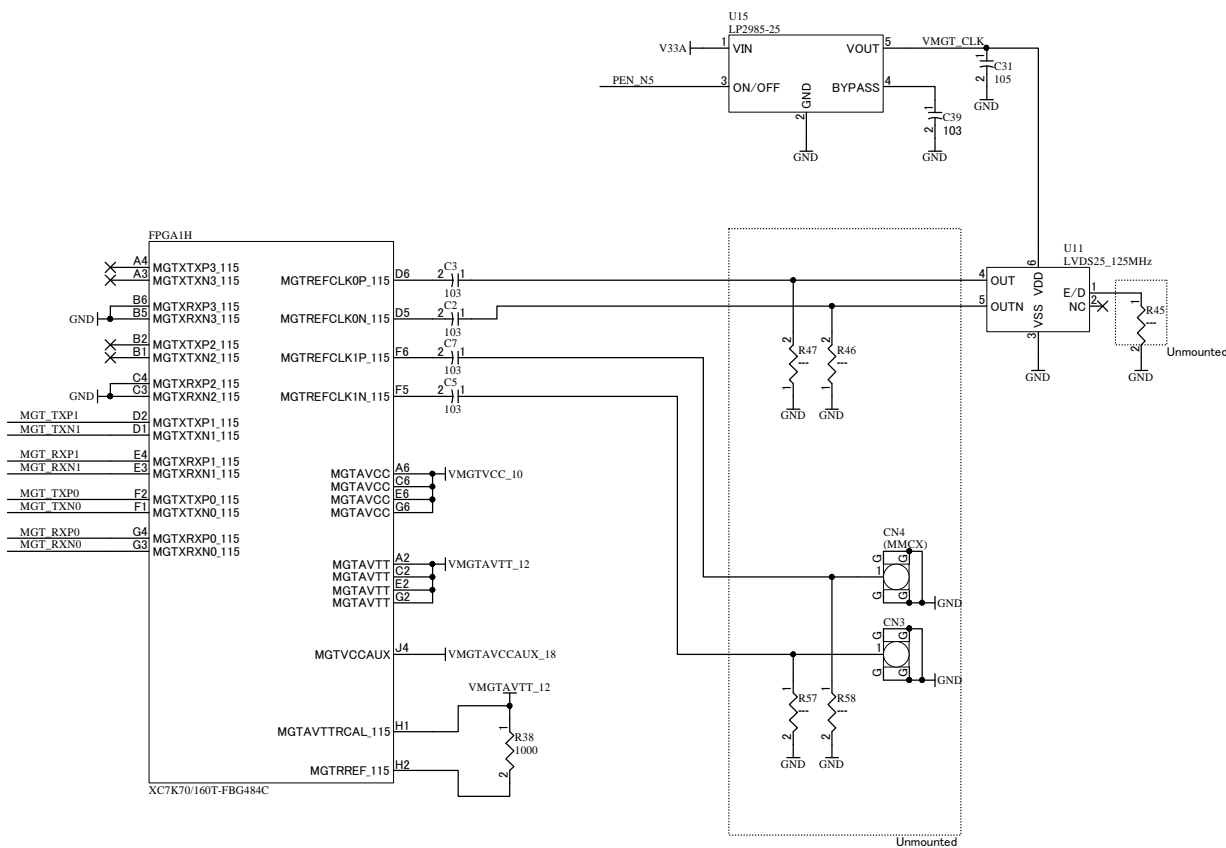
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		KINTEX FBG484 FPGA Board	
Date: 2014/09/22	16:12:30	File: XCM112_Memory.sch	Sheet 3 of 4

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VDDR_ORG	VDDR_ORG
VCCOA	VCCOA
VCCOB	VCCOB
VMGTAVCCAUX_18	VMGTAVCCAUX_18
VCCXADC_18	VCCXADC_18
GND	GND

MGT_TXP0	MGT_TXP0
MGT_TXN0	MGT_TXN0
MGT_RXP0	MGT_RXP0
MGT_RXN0	MGT_RXN0
MGT_TXP1	MGT_TXP1
MGT_TXN1	MGT_TXN1
MGT_RXP1	MGT_RXP1
MGT_RXN1	MGT_RXN1

PEN_N5	PEN_N5
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XCM112R1-SCH-B.pdf

		KINTEX FBG484 FPGA Board	
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