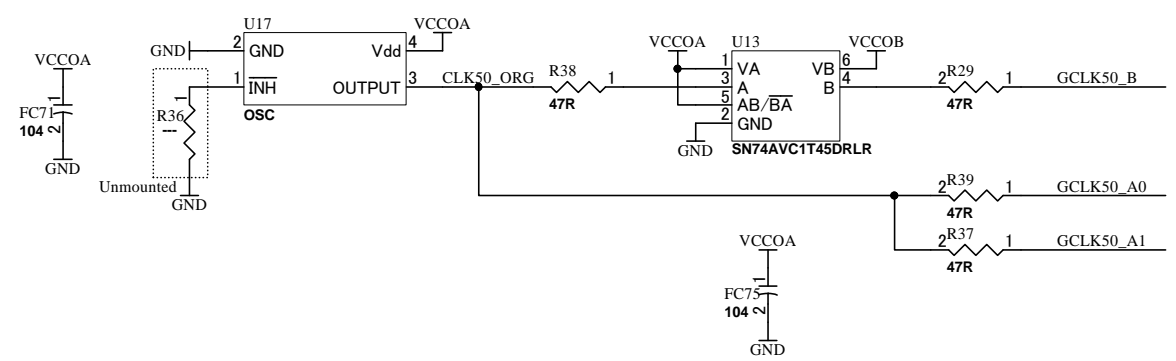
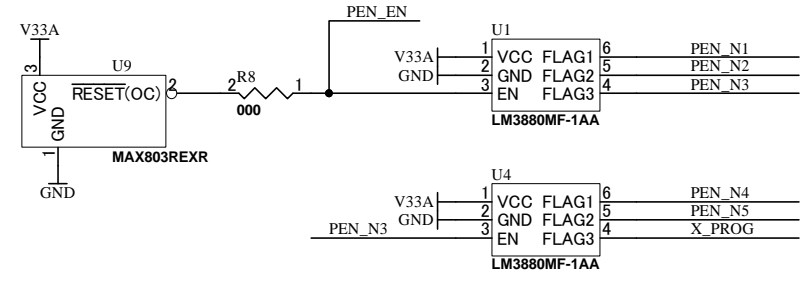
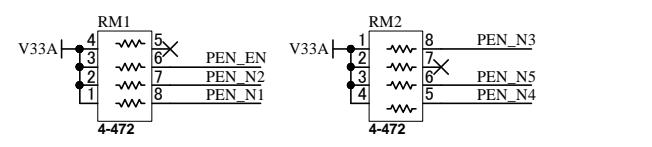
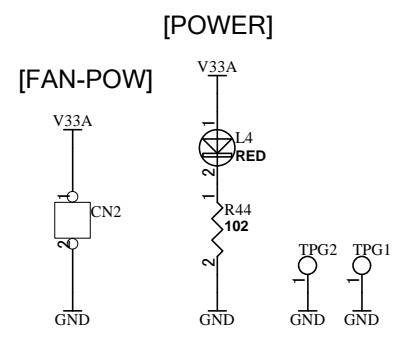
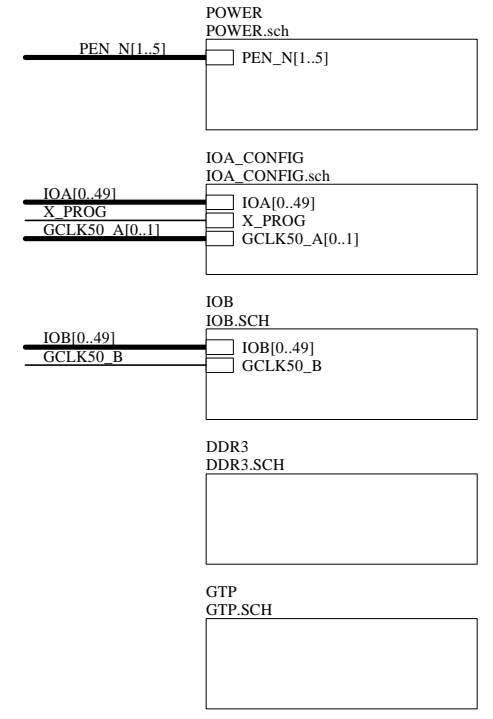
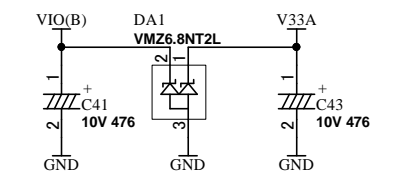


V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTVCC_10	VMGTVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VMGTCLK	VMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND

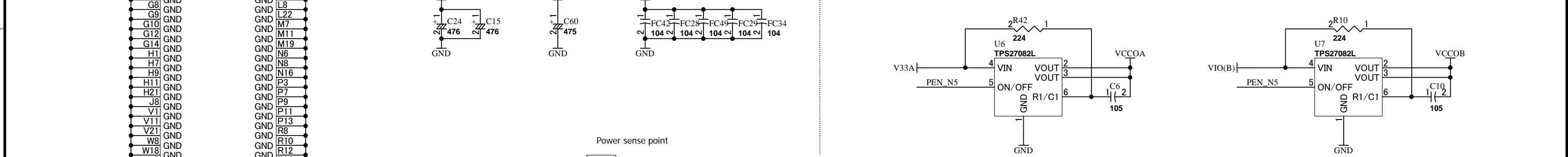
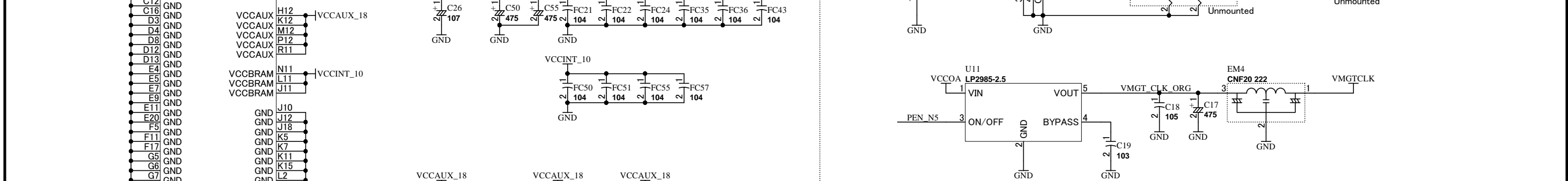
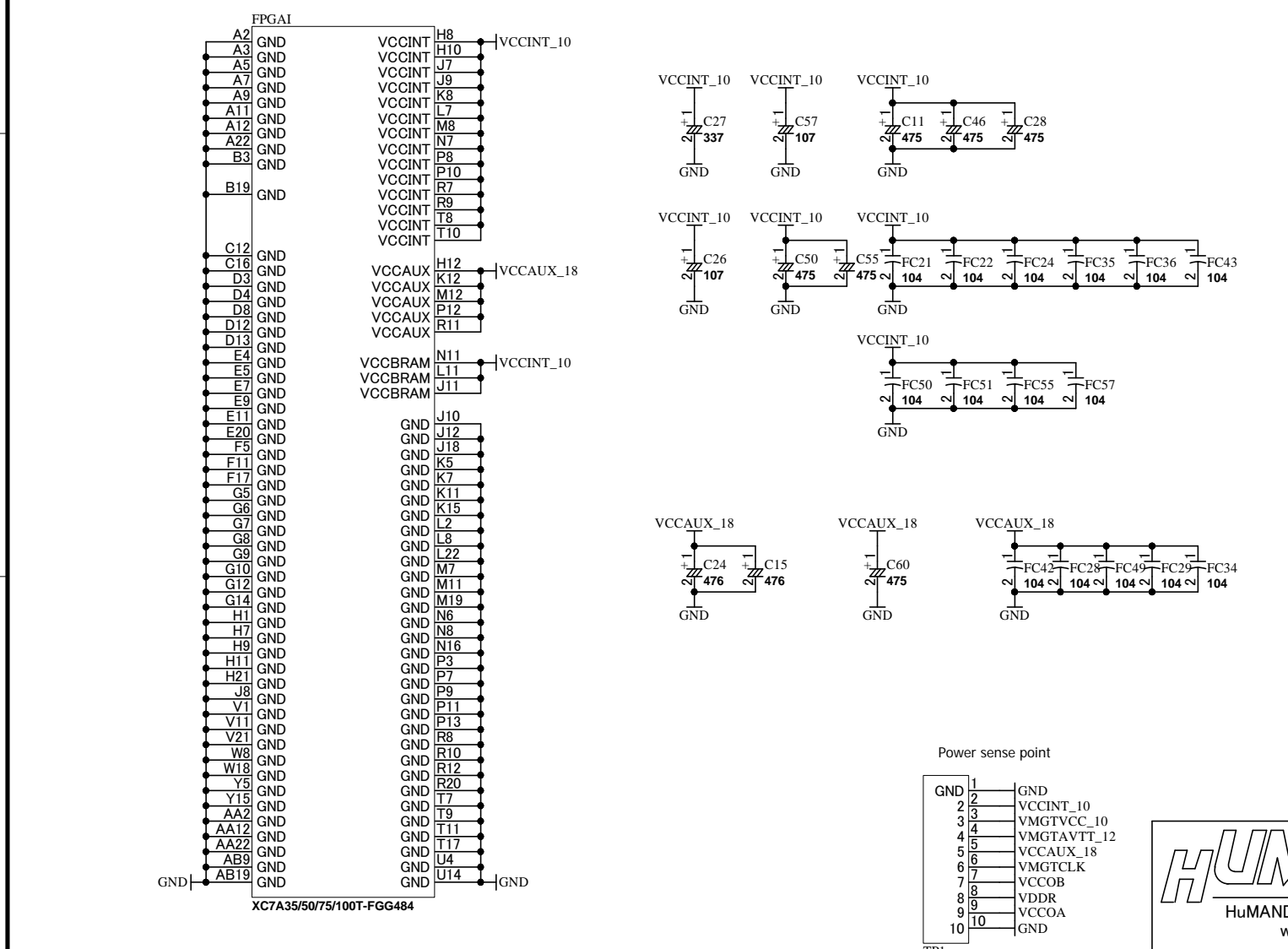
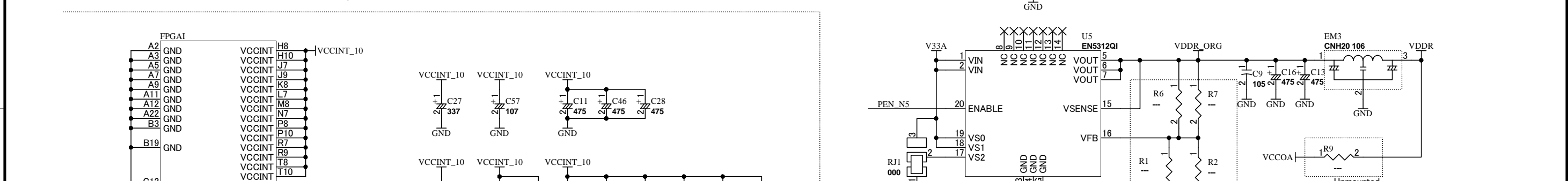
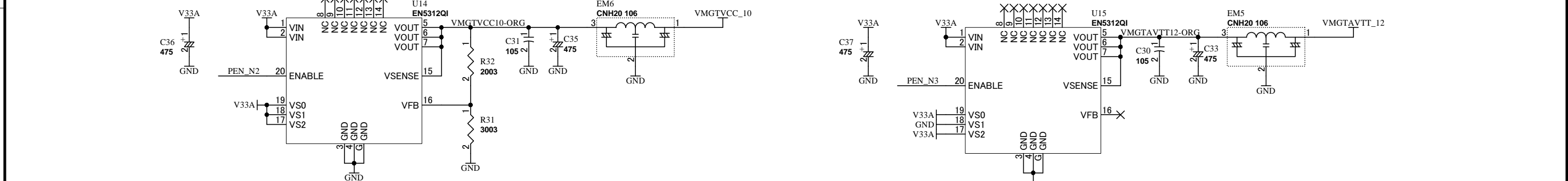
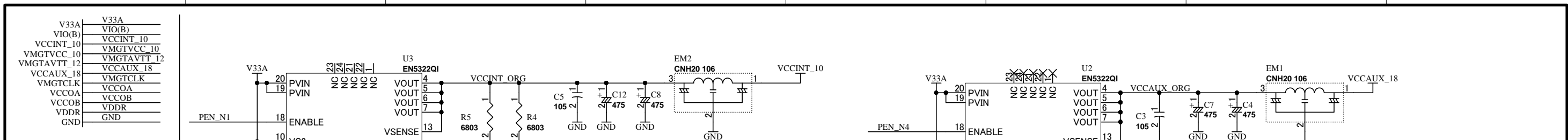


V33A	1	VIO(A)	1
GND	2	VIO(A)	2
IOA0	3	5V	3
IOA1	4	5V	4
IOA2	5	GND	5
IOA3	6	GND	6
IOA4	7	GND	7
IOA5	8	IOB0	8
IOA6	9	IOB1	9
IOA7	10	IOB2	10
IOA8	11	IOB3	11
IOA9	12	IOB4	12
IOA10	13	IOB5	13
IOA11	14	IOB6	14
IOA12	15	IOB7	15
IOA13	16	GND	16
IOA14	17	GND	17
IOA15	18	GND	18
GND	19	IOB8	19
GND	20	IOB9	20
IOA16	21	IOB10	21
IOA17	22	IOB11	22
IOA18	23	IOB12	23
IOA19	24	IOB13	24
IOA20	25	IOB14	25
IOA21	26	IOB15	26
IOA22	27	GND	27
IOA23	28	GND	28
GND	29	IOB16	29
IOA24	30	IOB17	30
IOA25	31	IOB18	31
IOA26	32	IOB19	32
IOA27	33	IOB20	33
IOA28	34	IOB21	34
IOA29	35	IOB22	35
IOA30	36	IOB23	36
IOA31	37	GND	37
GND	38	GND	38
GND	39	IOB24	39
IOA32	40	IOB25	40
IOA33	41	IOB26	41
IOA34	42	IOB27	42
IOA35	43	IOB28	43
IOA36	44	IOB29	44
IOA37	45	IOB30	45
IOA38	46	IOB31	46
IOA39	47	GND	47
GND	48	GND	48
GND	49	IOB32	49
IOA40	50	IOB33	50
IOA41	51	IOB34	51
IOA42	52	IOB35	52
IOA43	53	IOB36	53
IOA44	54	IOB37	54
IOA45	55	IOB38	55
IOA46	56	IOB39	56
IOA47	57	GND	57
IOA48	58	GND	58
IOA49	59	IOB40	59
	60	IOB41	60
	61	IOB42	61
	62	IOB43	62
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	65	IOB46	65
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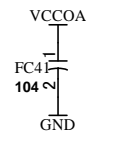
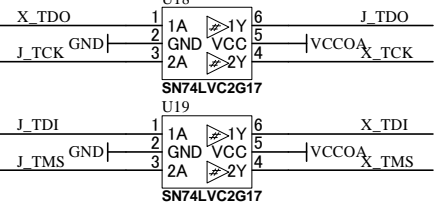
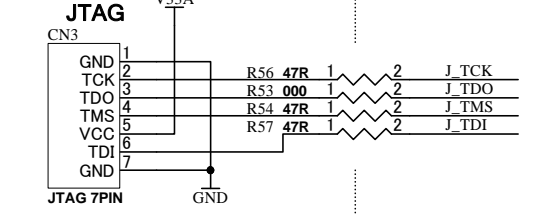
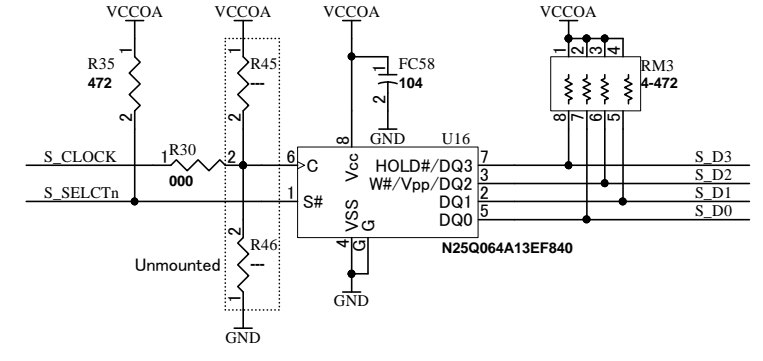
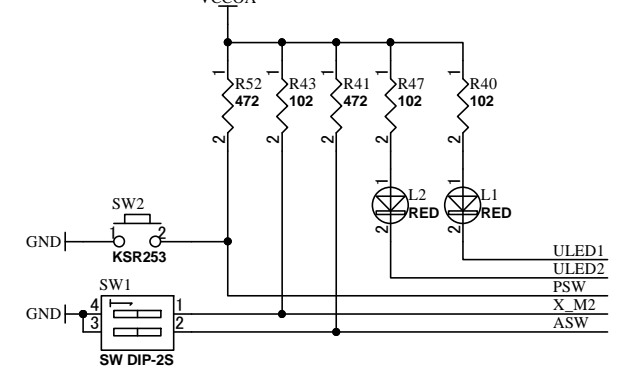
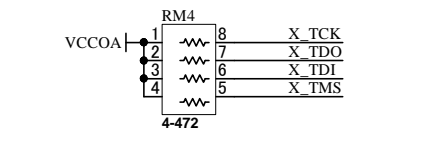
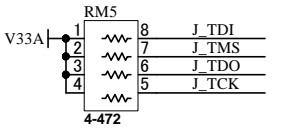
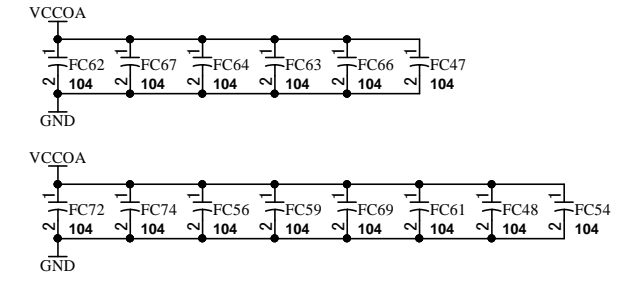
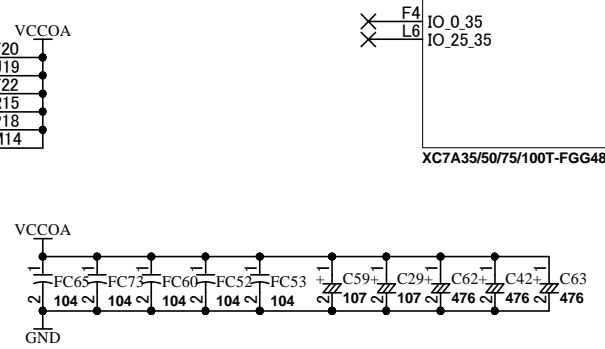
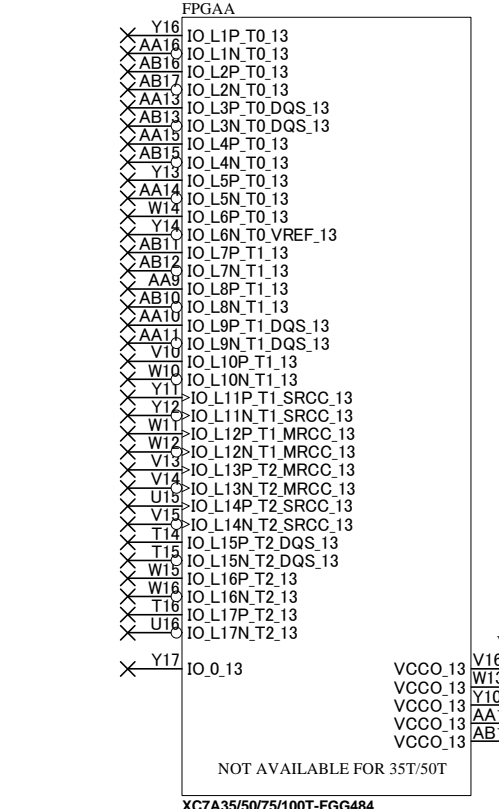
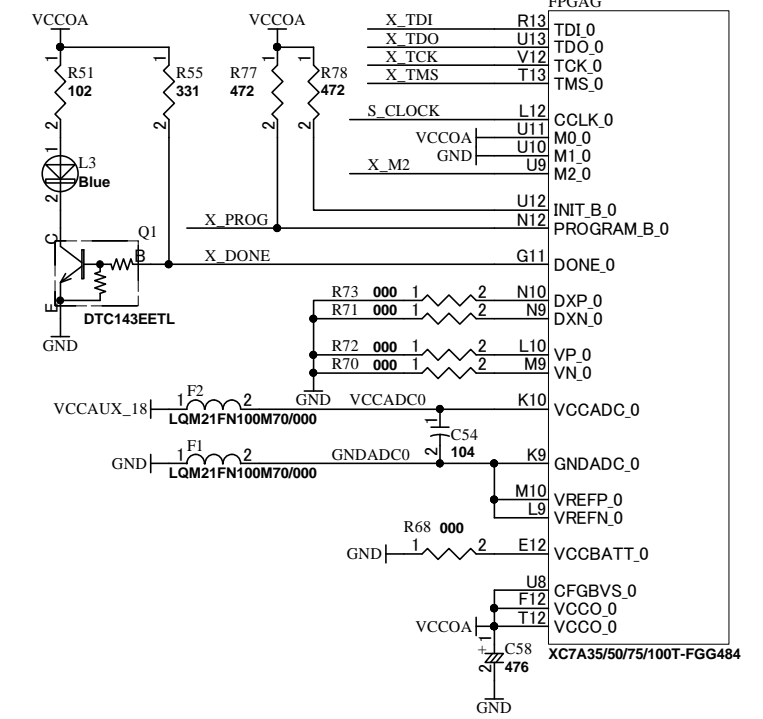
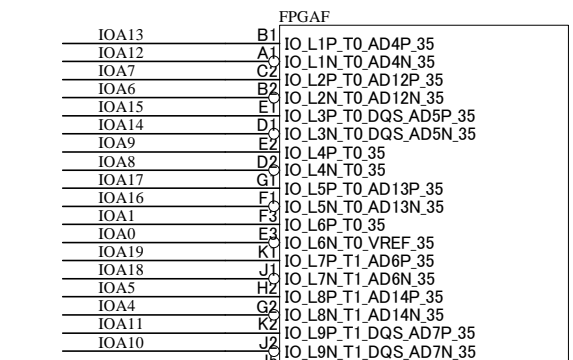
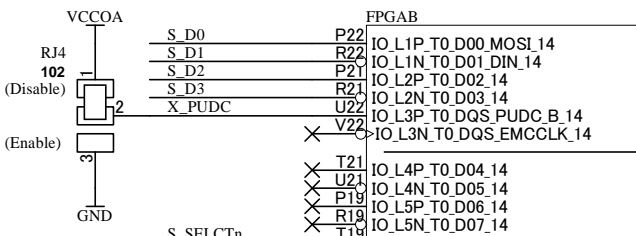
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	DOC. No. XCM-023	B
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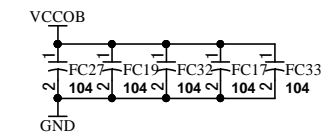
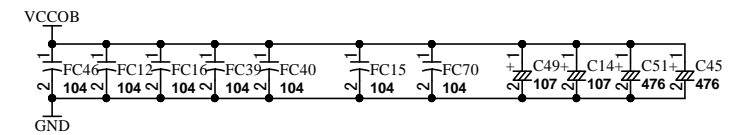
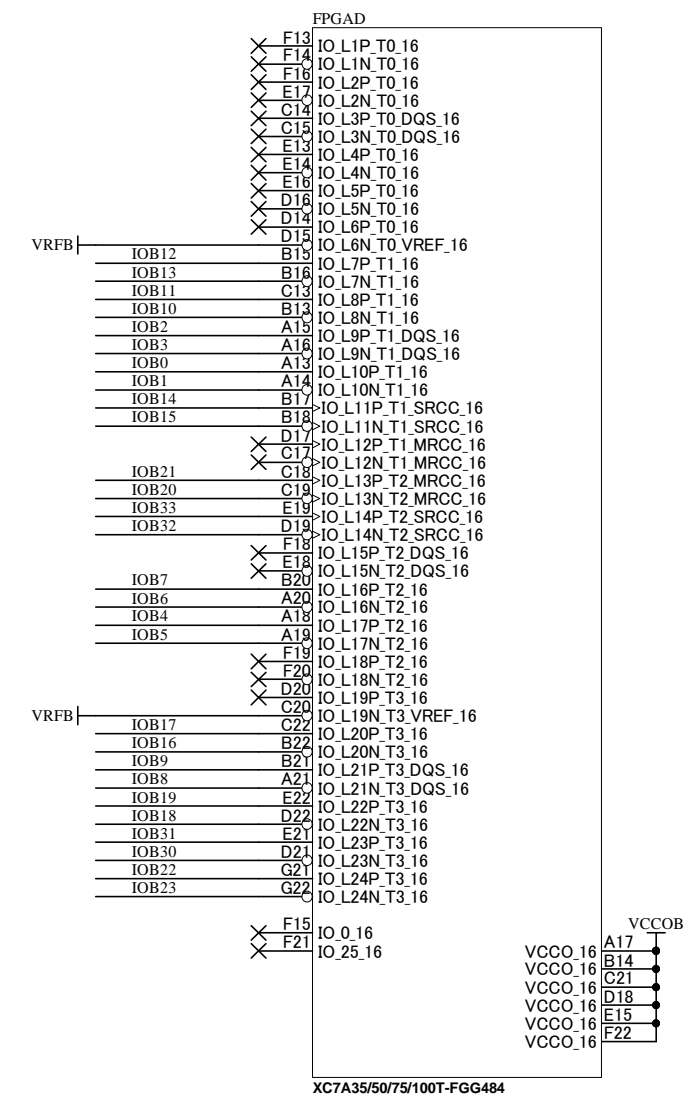
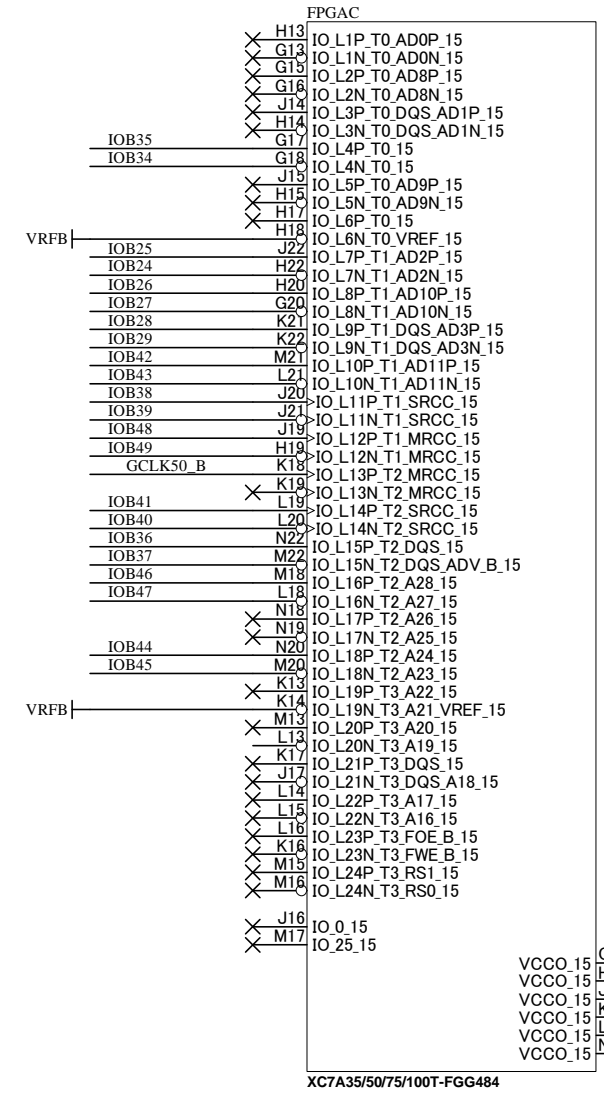
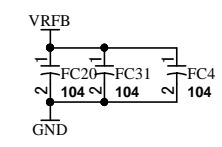
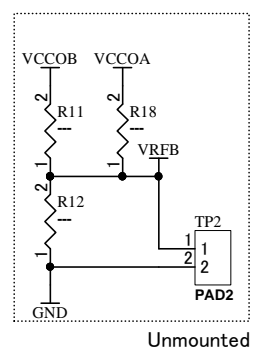
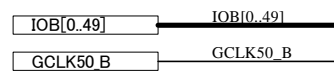
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		ARTIX-7 FGG484 FPGA Board	
		DOC. No. XCM-023	B

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTVCC_10	VMGTVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VMGTCLK	VMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND



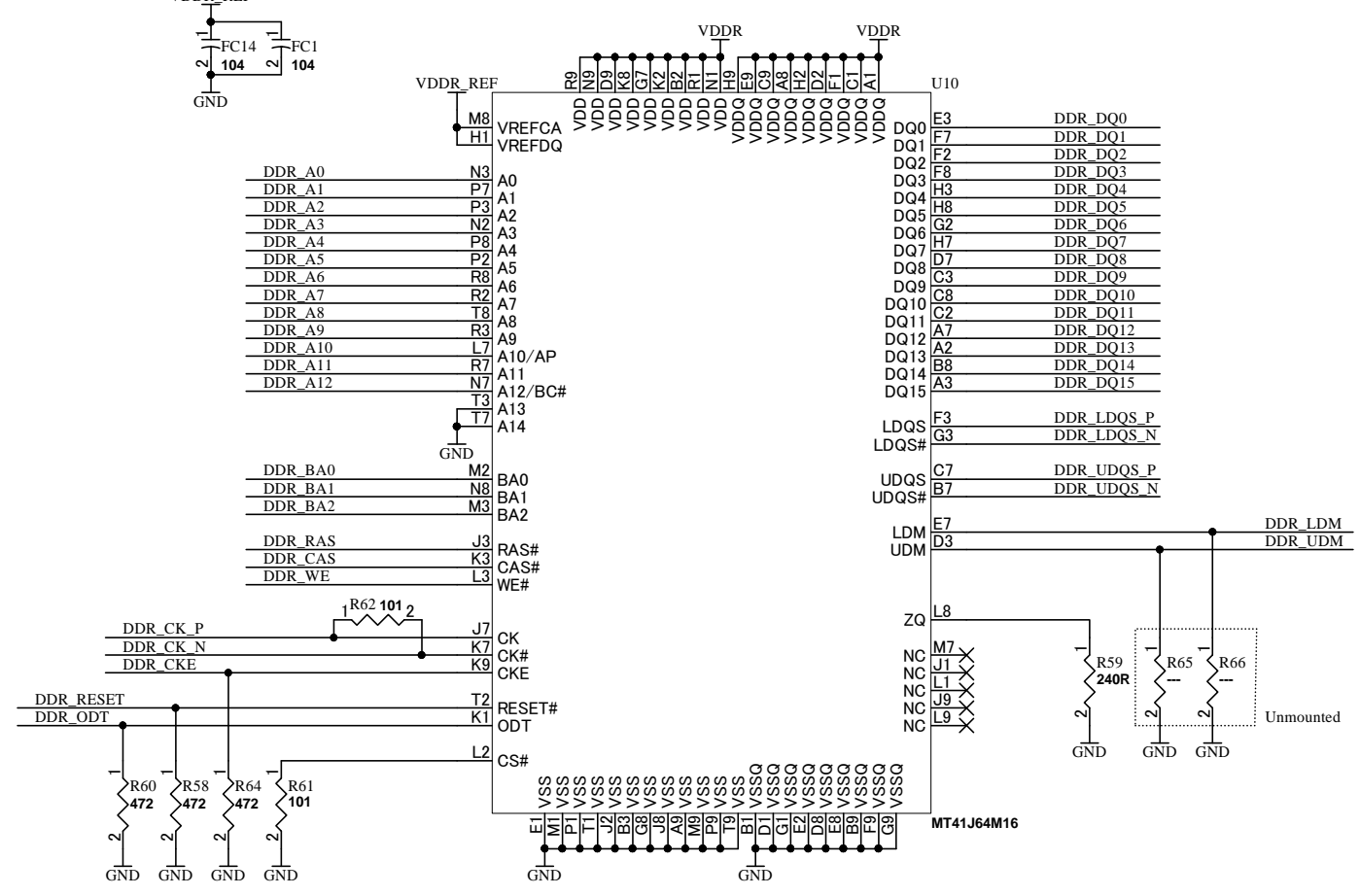
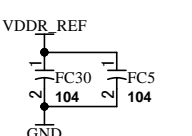
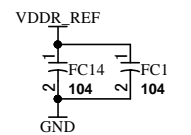
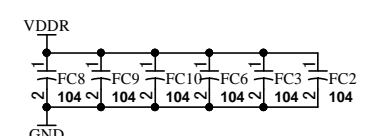
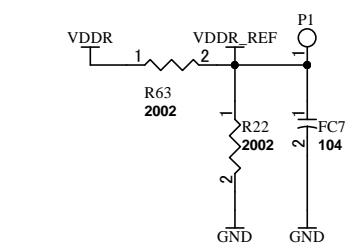
V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTVCC_10	VMGTVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VMGTCLK	VMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND



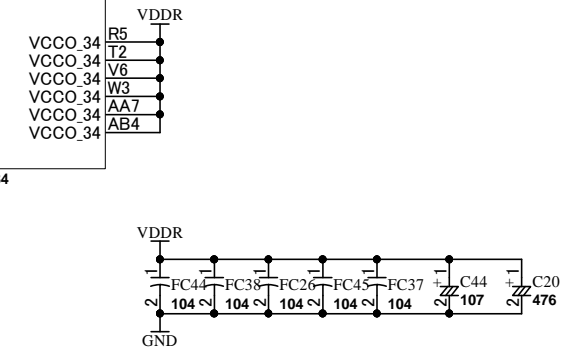
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<p>HUMAN DATA LTD. OSAKA JAPAN www.hdl.co.jp/en/(Global) www.hdl.co.jp/(Japan)</p>	ARTIX-7 FGG484 FPGA Board	
	DOC. No. XCM-023	B
Date: 2014/10/27	10:13:21 File: IOB.SCH	Sheet 4 of 6

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTVCC_10	VMGTVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VMGTCLK	VMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND



FPGA	
DDR_DQ6	T1
DDR_DQ4	U1
DDR_DQ0	U2
DDR_DQ7	V2
DDR_LDQS_P	R3
DDR_LDQS_N	R2
DDR_DQ1	W2
DDR_LDM	Y2
DDR_DQ5	W1
DDR_DQ3	Y1
DDR_DQ2	U3
VDDR_REF	V3
DDR_DQ11	AA1
DDR_DQ9	AB1
DDR_DQ8	AB3
DDR_UDM	AB2
DDR_UDQS_P	V3
DDR_UDQS_N	AA3
DDR_DQ14	AA5
DDR_DQ10	AB5
DDR_DQ13	Y4
DDR_DQ12	AA4
DDR_DQ15	V4
DDR_RESET	W4
DDR_CKE	R4
DDR_CAS	T4
DDR_A3	T5
DDR_BA2	U5
DDR_ODT	W6
DDR_WE	W5
DDR_A5	U6
DDR_BA0	V5
DDR_A7	R6
DDR_A2	T6
DDR_A10	Y6
DDR_A6	AA6
DDR_A12	V7
VDDR_REF	W7
DDR_A11	AB7
DDR_A8	AB6
DDR_CK_P	V9
DDR_CK_N	V8
DDR_A1	AA8
DDR_BA1	AB8
DDR_RAS	Y8
DDR_A4	Y7
DDR_A0	W9
DDR_A9	V9
IO_0_34	T3
IO_25_34	U7

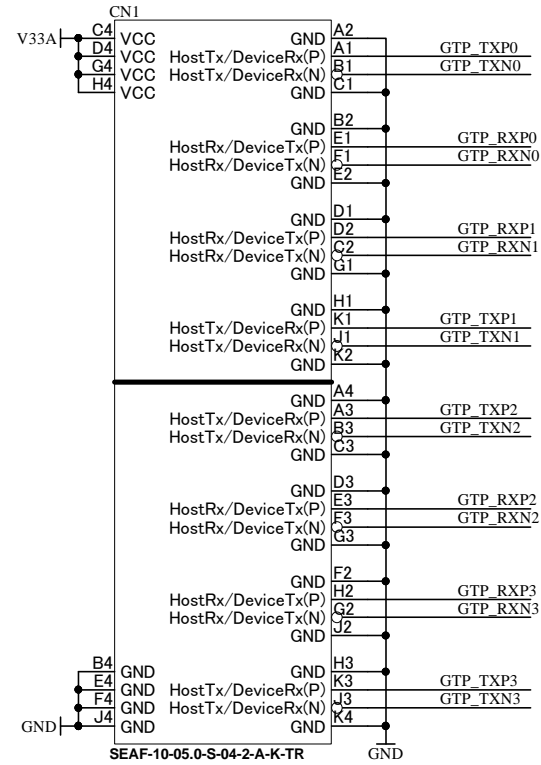


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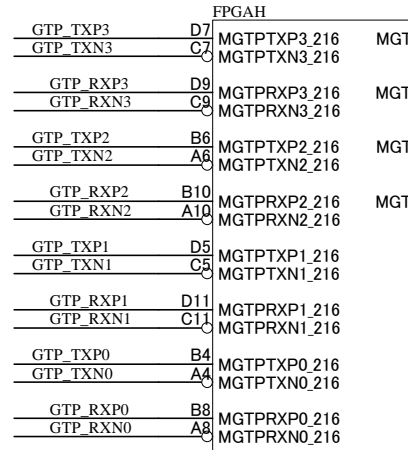
<p>HUMAN DATA LTD. OSAKA JAPAN www.hdl.co.jp/en/(Global) www.hdl.co.jp/(Japan)</p>	ARTIX-7 FGG484 FPGA Board	
	DOC. No. XCM-023	B
Date: 2014/10/27	10:13:21 File: DDR3.SCH	Sheet 5 of 6

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVCC_10	VMGTAVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VMGTCLK	VMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND

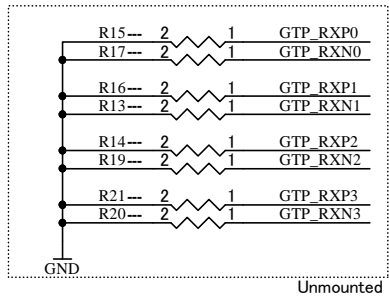
SIF40 (Receptacle)



SEAF-10-05.0-S-04-2-A-K-TR



XC7A35/50/75/100T-FGG484



Unmounted

