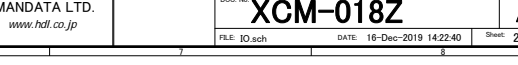
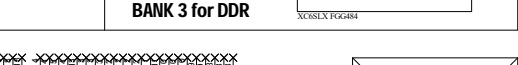
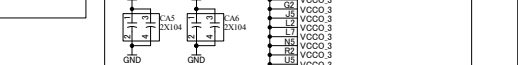
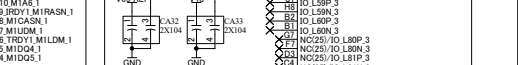
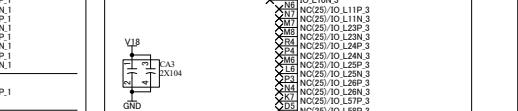
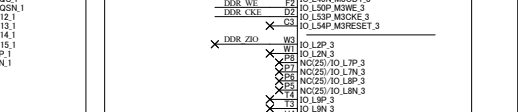
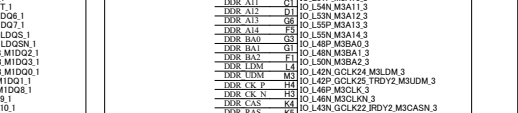
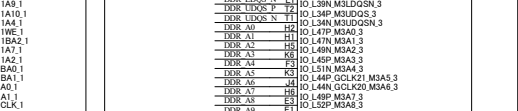
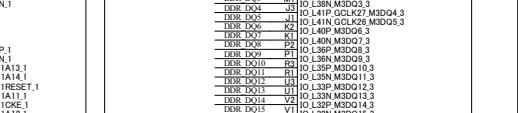
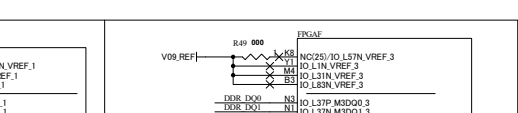
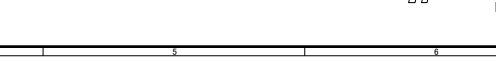
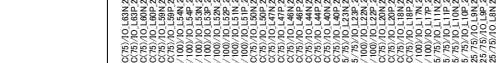
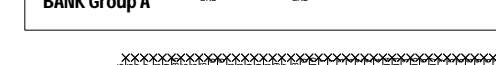
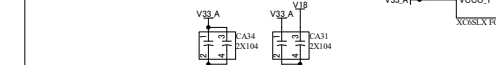
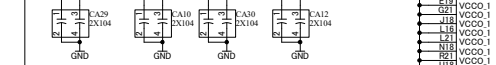
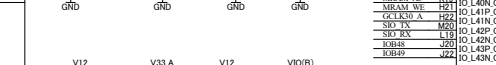
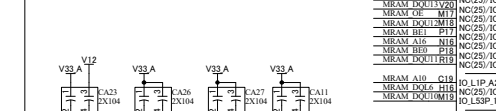
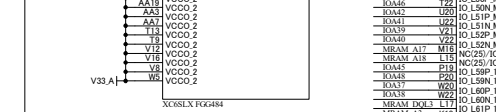
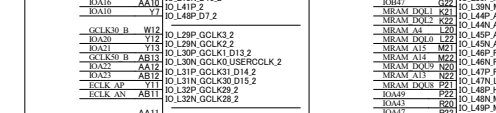
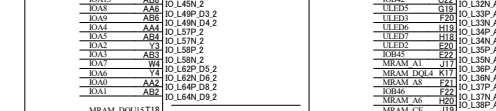
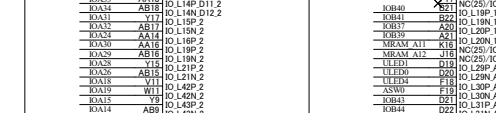
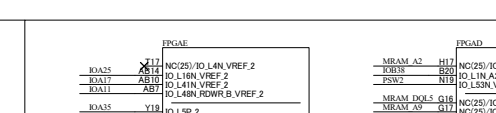
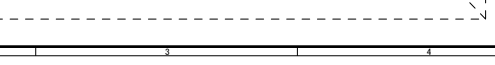
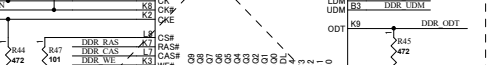
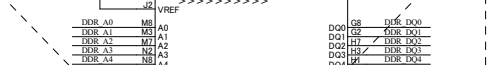
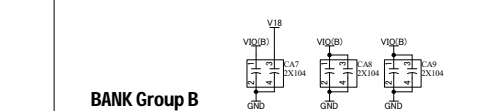
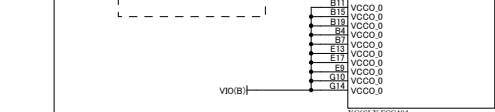
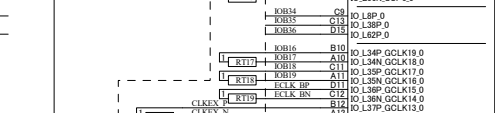
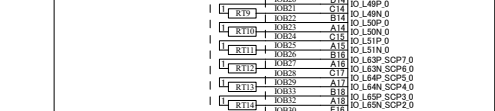
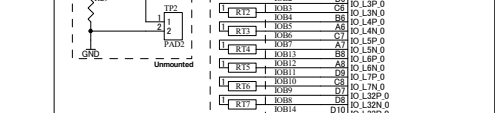
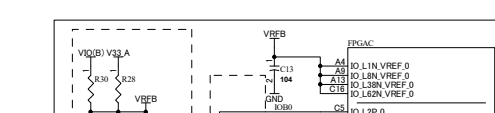
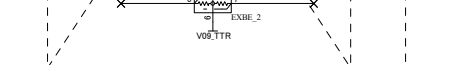
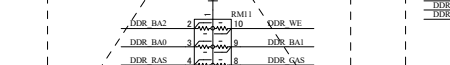
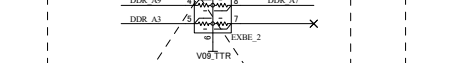
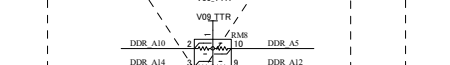
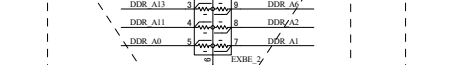
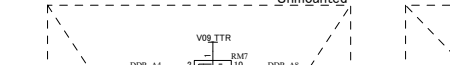
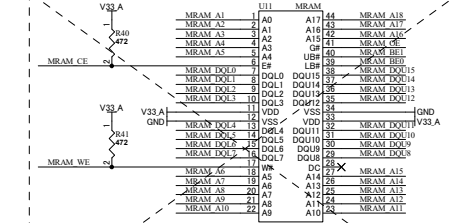
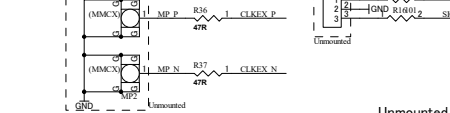
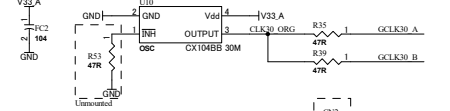
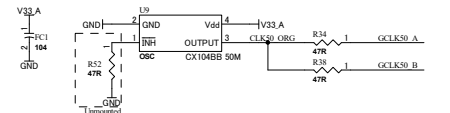
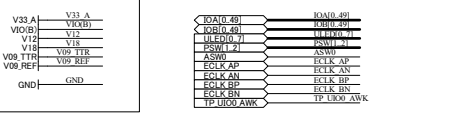


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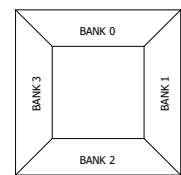
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**BANK Group B**

**BANK Group A**

**BANK 3 for DDR**



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SPARTAN-6 FG484 FPGA Board

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**A5**

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