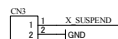
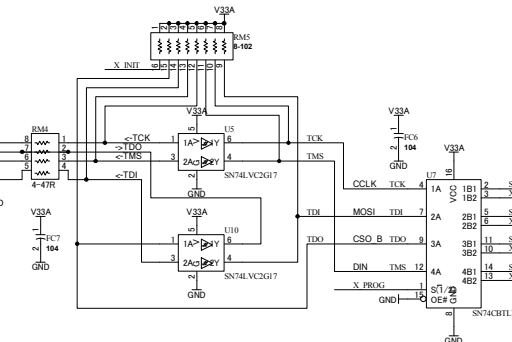
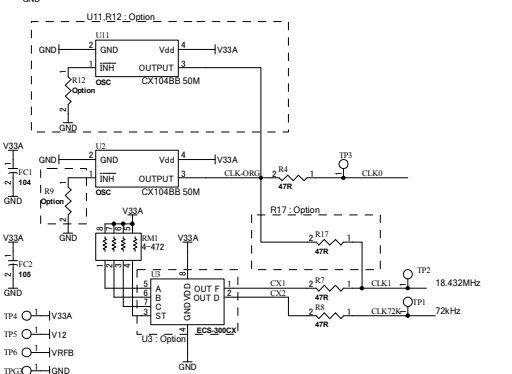
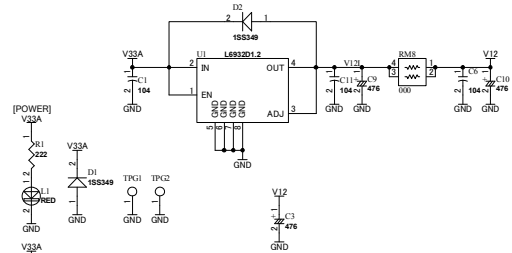
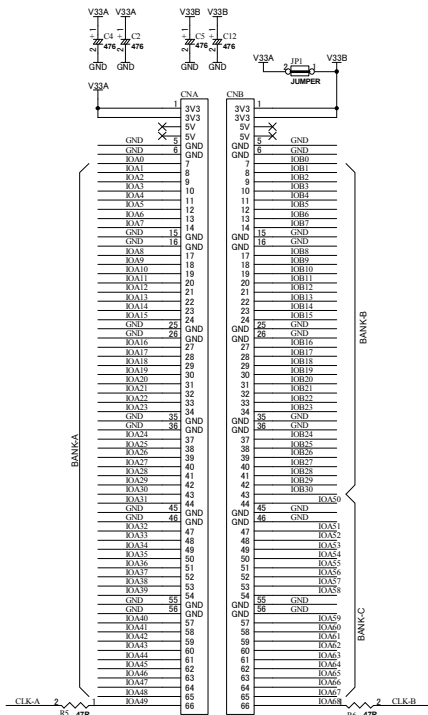
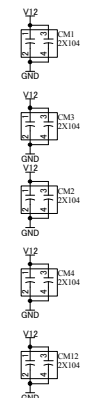


Vaux1
V33A
V33B
V12
GND

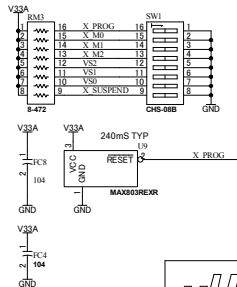
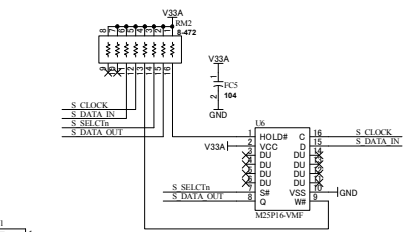


[xxx] is FPGA PIN NAME of 700/1400

FPGA	VCCALX(VCCALX)	E11	Vaux
A1	GND	F5	Vaux
A16	GND	F6	Vaux
A31	GND	F7	Vaux
A47	GND	F8	Vaux
A63	GND	F9	Vaux
A79	GND	F10	Vaux
A95	GND	F11	Vaux
A111	GND	F12	Vaux
A127	GND	F13	Vaux
A143	GND	F14	Vaux
A159	GND	F15	Vaux
A175	GND	F16	Vaux
A191	GND	F17	Vaux
A207	GND	F18	Vaux
A223	GND	F19	Vaux
A239	GND	F20	Vaux
A255	GND	F21	Vaux
A271	GND	F22	Vaux
A287	GND	F23	Vaux
A303	GND	F24	Vaux
A319	GND	F25	Vaux
A335	GND	F26	Vaux
A351	GND	F27	Vaux
A367	GND	F28	Vaux
A383	GND	F29	Vaux
A399	GND	F30	Vaux
A415	GND	F31	Vaux
A431	GND	F32	Vaux
A447	GND	F33	Vaux
A463	GND	F34	Vaux
A479	GND	F35	Vaux
A495	GND	F36	Vaux
A511	GND	F37	Vaux
A527	GND	F38	Vaux
A543	GND	F39	Vaux
A559	GND	F40	Vaux
A575	GND	F41	Vaux
A591	GND	F42	Vaux
A607	GND	F43	Vaux
A623	GND	F44	Vaux
A639	GND	F45	Vaux
A655	GND	F46	Vaux
A671	GND	F47	Vaux
A687	GND	F48	Vaux
A703	GND	F49	Vaux
A719	GND	F50	Vaux
A735	GND	F51	Vaux
A751	GND	F52	Vaux
A767	GND	F53	Vaux
A783	GND	F54	Vaux
A799	GND	F55	Vaux
A815	GND	F56	Vaux
A831	GND	F57	Vaux
A847	GND	F58	Vaux
A863	GND	F59	Vaux
A879	GND	F60	Vaux
A895	GND	F61	Vaux
A911	GND	F62	Vaux
A927	GND	F63	Vaux
A943	GND	F64	Vaux
A959	GND	F65	Vaux
A975	GND	F66	Vaux
A991	GND	F67	Vaux
A1007	GND	F68	Vaux
A1023	GND	F69	Vaux
A1039	GND	F70	Vaux
A1055	GND	F71	Vaux
A1071	GND	F72	Vaux
A1087	GND	F73	Vaux
A1103	GND	F74	Vaux
A1119	GND	F75	Vaux
A1135	GND	F76	Vaux
A1151	GND	F77	Vaux
A1167	GND	F78	Vaux
A1183	GND	F79	Vaux
A1199	GND	F80	Vaux
A1215	GND	F81	Vaux
A1231	GND	F82	Vaux
A1247	GND	F83	Vaux
A1263	GND	F84	Vaux
A1279	GND	F85	Vaux
A1295	GND	F86	Vaux
A1311	GND	F87	Vaux
A1327	GND	F88	Vaux
A1343	GND	F89	Vaux
A1359	GND	F90	Vaux
A1375	GND	F91	Vaux
A1391	GND	F92	Vaux
A1407	GND	F93	Vaux
A1423	GND	F94	Vaux
A1439	GND	F95	Vaux
A1455	GND	F96	Vaux
A1471	GND	F97	Vaux
A1487	GND	F98	Vaux
A1503	GND	F99	Vaux
A1519	GND	F100	Vaux



FPGA	SUSPEND[SUSPEND]	R16	X_SUSPEND
A16	SUSPEND[SUSPEND]	R16	X_SUSPEND
A32	DONE[DONE]	R17	DONE[DONE]
A48	PROG_B[PROG_B]	R18	PROG_B[PROG_B]
A64	TD0[TD0]	R19	TD0[TD0]
A80	TD1[TD1]	R20	TD1[TD1]
A96	TD2[TD2]	R21	TD2[TD2]
A112	TMS[TMS]	R22	TMS[TMS]

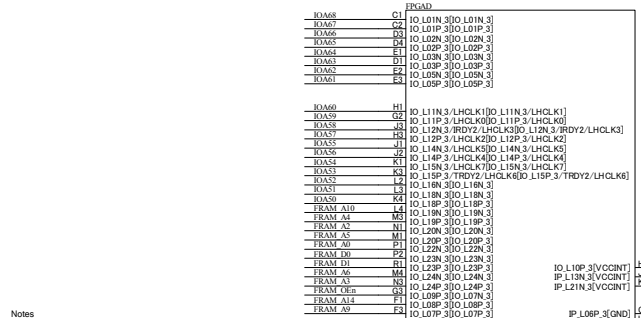
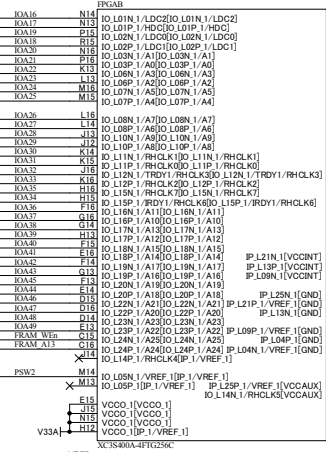
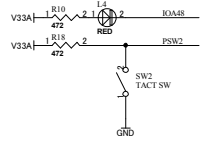
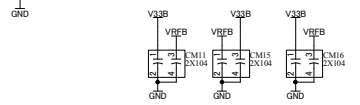
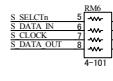
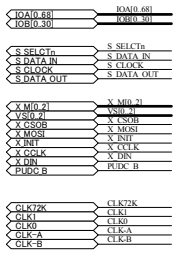
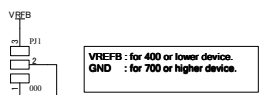
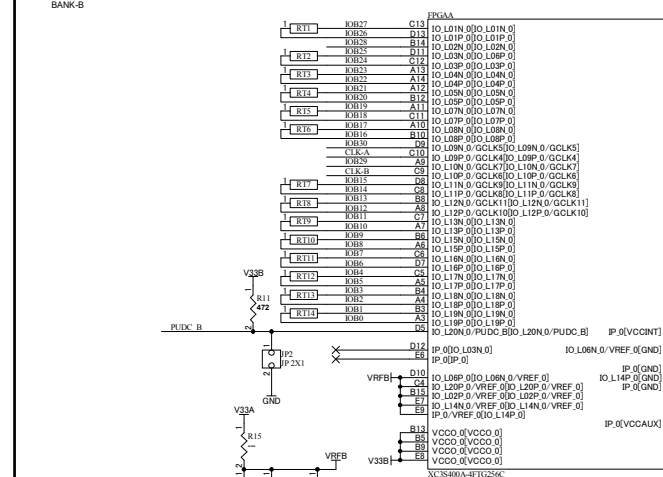
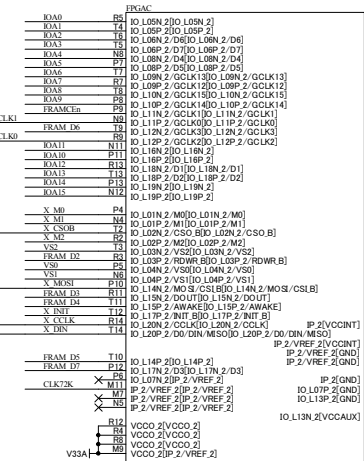


IO	R3 sch
IOA[0..68]	IOA[0..68]
IOB[0..30]	IOB[0..30]
S_SELECT_B	S_SELECT_B
S_SELECT_A	S_SELECT_A
S_CLOCK	S_CLOCK
S_DATA_IN	S_DATA_IN
S_DATA_OUT	S_DATA_OUT
VSS0_0	VSS0_0
VSS0_1	VSS0_1
VSS0_2	VSS0_2
VSS0_3	VSS0_3
VSS0_4	VSS0_4
VSS0_5	VSS0_5
VSS0_6	VSS0_6
VSS0_7	VSS0_7
VSS0_8	VSS0_8
VSS0_9	VSS0_9
VSS0_10	VSS0_10
VSS0_11	VSS0_11
VSS0_12	VSS0_12
VSS0_13	VSS0_13
VSS0_14	VSS0_14
VSS0_15	VSS0_15
VSS0_16	VSS0_16
VSS0_17	VSS0_17
VSS0_18	VSS0_18
VSS0_19	VSS0_19
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VSS0_68	VSS0_68
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VSS0_76	VSS0_76
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VSS0_80	VSS0_80
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VSS0_82	VSS0_82
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VSS0_94	VSS0_94
VSS0_95	VSS0_95
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VSS0_98	VSS0_98
VSS0_99	VSS0_99

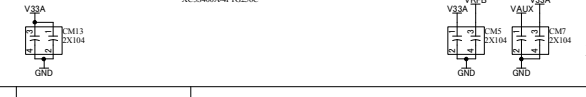
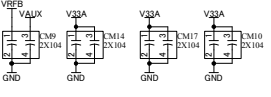
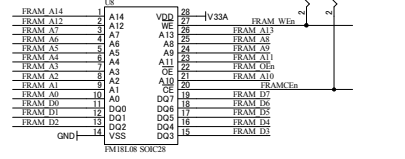
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Vaux V33A
V33B V33B
V12 V12
GND GND

[xxx] is FPGA PIN NAME of 700/1400



FPGA Part	FRAM_A8	FRAM_A11
XC3S400A	J4	G4
XC3S700A/1400A	E4	F4



	2009/11/25	Xilinx Spartan-3A FTG256 FPGA board	DOC. No.	XCM-014	A3
	HuMANDATA LTD. OSAKA JAPAN www.hdl.co.jp/en/(Global) www.hdl.co.jp/(Japan)				

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