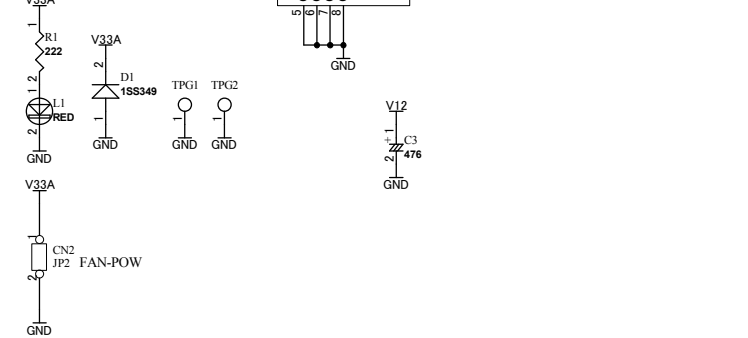
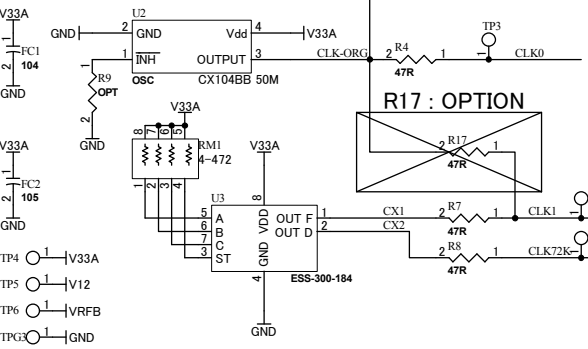
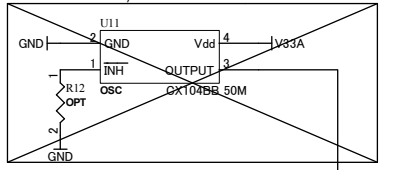


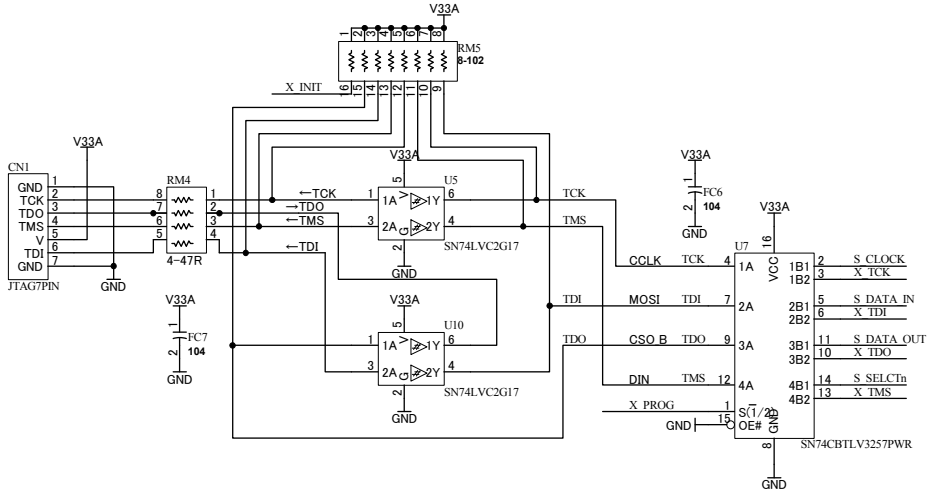
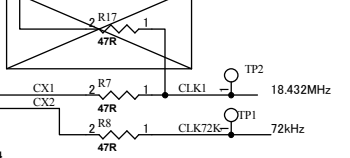
[POWER]



U11,R12 : OPTION

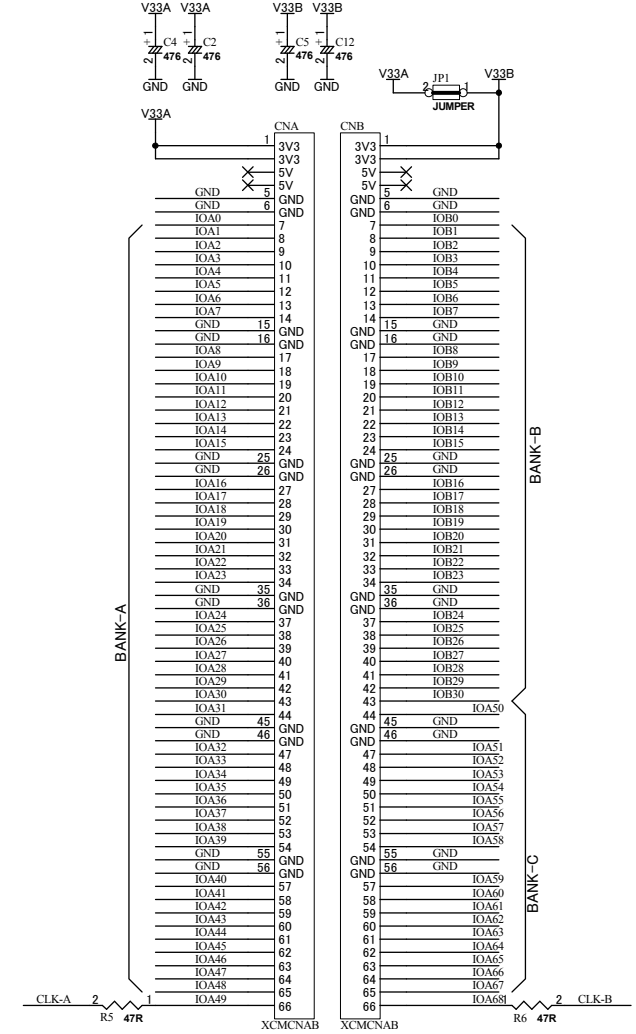
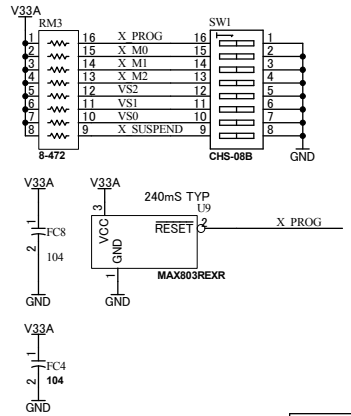
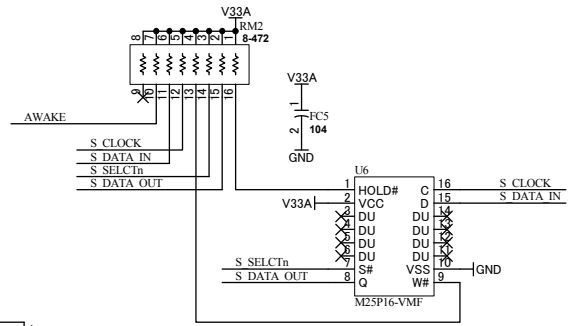
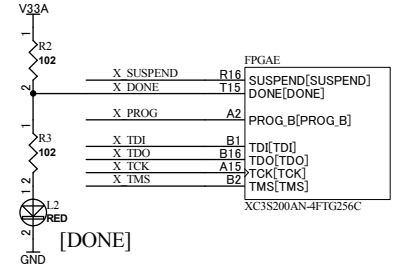


R17 : OPTION

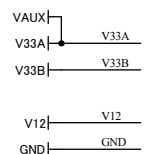


[xxx]は700/1400のFPGA PIN NAME

FPGA	VCC(AUX)(VCCAUX)	V12
A1	GND	G7
A16	GND	G8
B1	GND	G9
B7	GND	G10
C3	GND	G11
E12	GND	G12
F5	GND	G13
F6	GND	G14
F8	GND	G15
G10	GND	G16
G15	GND	G17
H9	GND	G18
J8	GND	G19
K2	GND	G20
K7	GND	G21
K9	GND	G22
L11	GND	G23
L15	GND	G24
M5	GND	G25
M12	GND	G26
P3	GND	G27
P14	GND	G28
R6	GND	G29
R10	GND	G30
T1	GND	G31
T16	GND	G32
GND	GND	G33
GND	GND	G34
GND	GND	G35
GND	GND	G36
GND	GND	G37
GND	GND	G38
GND	GND	G39
GND	GND	G40
GND	GND	G41
GND	GND	G42
GND	GND	G43
GND	GND	G44
GND	GND	G45
GND	GND	G46
GND	GND	G47
GND	GND	G48
GND	GND	G49
GND	GND	G50
GND	GND	G51
GND	GND	G52
GND	GND	G53
GND	GND	G54
GND	GND	G55
GND	GND	G56
GND	GND	G57
GND	GND	G58
GND	GND	G59
GND	GND	G60
GND	GND	G61
GND	GND	G62
GND	GND	G63
GND	GND	G64
GND	GND	G65
GND	GND	G66
GND	GND	G67
GND	GND	G68
GND	GND	G69
GND	GND	G70
GND	GND	G71
GND	GND	G72
GND	GND	G73
GND	GND	G74
GND	GND	G75
GND	GND	G76
GND	GND	G77
GND	GND	G78
GND	GND	G79
GND	GND	G80
GND	GND	G81
GND	GND	G82
GND	GND	G83
GND	GND	G84
GND	GND	G85
GND	GND	G86
GND	GND	G87
GND	GND	G88
GND	GND	G89
GND	GND	G90
GND	GND	G91
GND	GND	G92
GND	GND	G93
GND	GND	G94
GND	GND	G95
GND	GND	G96
GND	GND	G97
GND	GND	G98
GND	GND	G99
GND	GND	G100

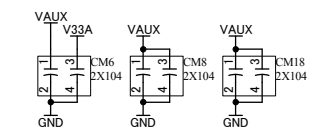
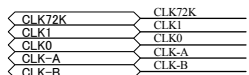
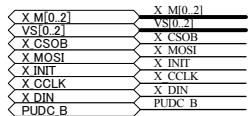
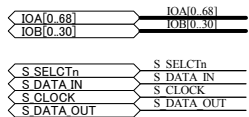


IO	IO_sch
IOA[0..68]	IOA[0..68]
IOB[0..30]	IOB[0..30]
S_SELECTn	S_SELECTn
S_DATA IN	S_DATA IN
S_CLOCK	S_CLOCK
X_MIO[2]	X_MIO[2]
S_DATA OUT	VS[0..2]
X_CS0B	S_DATA_OUT
X_MOSI	X_CS0B
AWAKE	X_MOSI
X_INIT	AWAKE
X_CCLK	X_INIT
X_DIN	X_CCLK
PUDC_B	X_DIN
CLK72K	PUDC_B
CLK1	CLK72K
CLK0	CLK1
CLK-A	CLK0
CLK-B	CLK-A



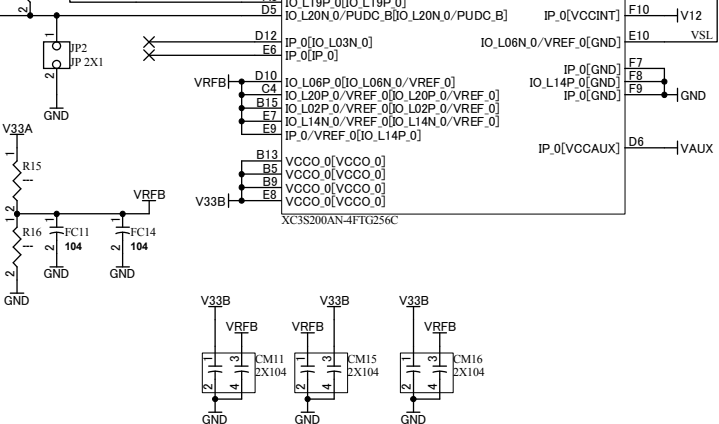
[xxx]は700/1400のFPGA PIN NAME

Table listing FPGA pins (IOA0 to IOA15, etc.) and their configurations (IO L05N 2, IO L05P 2, etc.) for the XC3S200AN-4FTG256C.



BANK-B

Table listing FPGA pins (IOB27 to IOB11, etc.) and their configurations for Bank B.



FPGA PIN [E10]は400以下のデバイスの時1/0またはVREFで700以上のときGNDです。そのため以下のように0Ω抵抗を実装しています。

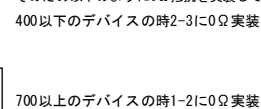
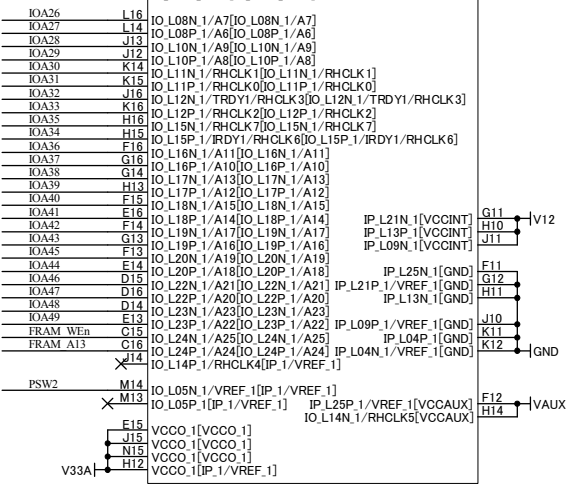
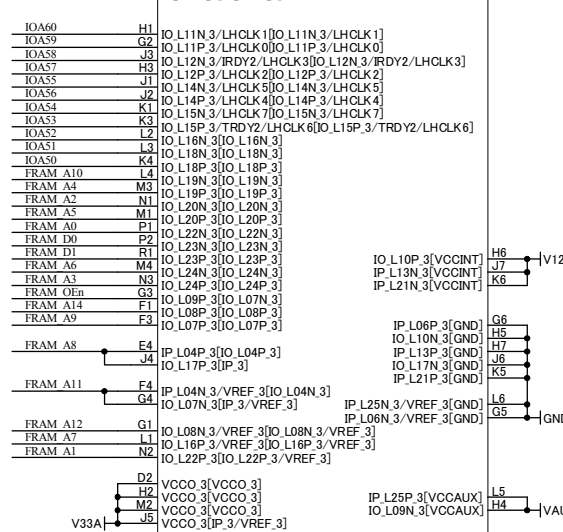


Table listing FPGA pins (IOA16 to IOA25, IOA26 to IOA32, etc.) and their configurations for the XC3S200AN-4FTG256C.



BANK-C

Table listing FPGA pins (IOA68 to IOA61, IOA60 to IOA53, etc.) and their configurations for Bank C.



FRAM使用時の注意

Table showing FRAM_A8 and FRAM_A11 configurations for 400使用時 (J4, G4) and 700/1400使用時 (E4, F4).

