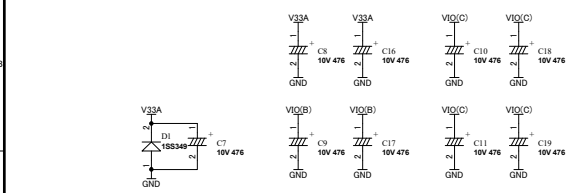
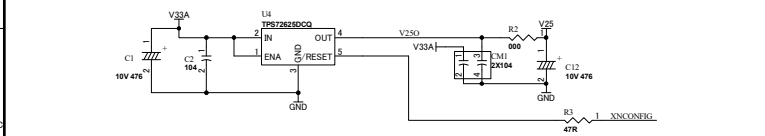
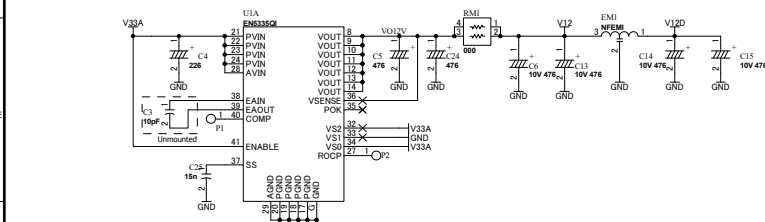
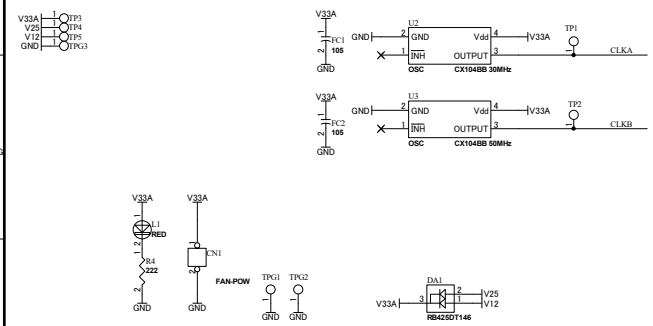


Pin definition table for V12, V12D, V25, V33A, V33A, VIO(B), VIO(C), GND.



Pin list for FPGA1 (FPGA1sch) with connections to VCCINT, GND, and V12.

Pin list for FPGA2 (FPGA2sch) with connections to VCCINT, GND, and V12. Includes a note: 'These pins are connected to GND or VCCINT. You need to set them as INPUT.'

Pin list for FPGA1 (FPGA1sch) with connections to IOA[0..8], CLKA, XNCONFIG, CLK0, CLK1, and IOG[0..83].

Pin list for FPGA2 (FPGA2sch) with connections to IOB[0..83], IOG[0..83], IOG[0..31], CLK2, CLK3, CLK4, CLK5, CLK6, CLK7, CLK8, CLK9, CLK10, and CLK11.

Pin list for FPGA1 (FPGA1sch) with connections to V33A, VIO(B), and VIO(C). Includes notes about bank groups.

Pin list for FPGA2 (FPGA2sch) with connections to V33A, VIO(B), and VIO(C). Includes notes about bank groups.

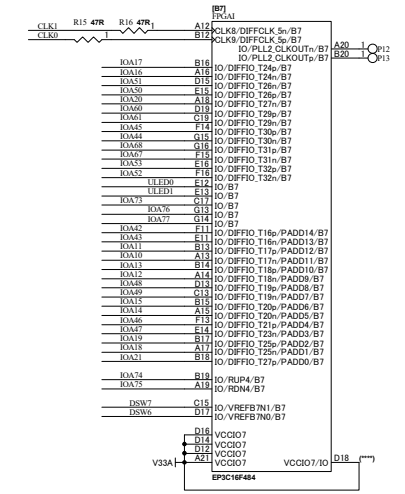
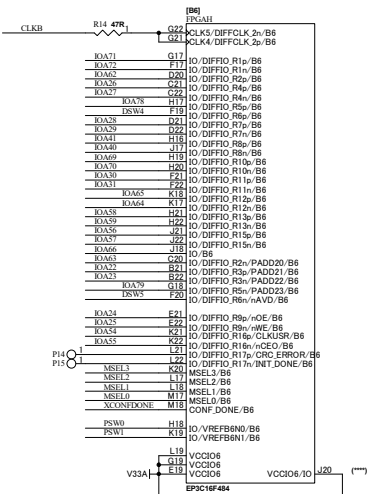
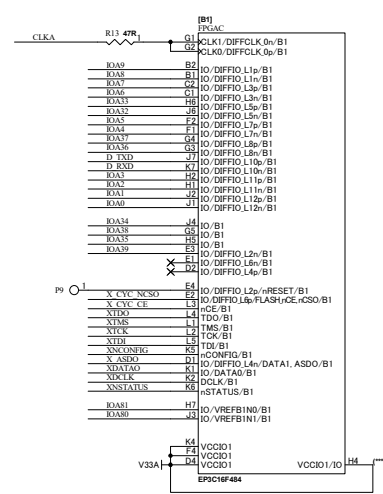
Pin list for FPGA1 (FPGA1sch) with connections to VIO(B) and VIO(C).

Pin list for FPGA2 (FPGA2sch) with connections to VIO(B) and VIO(C).

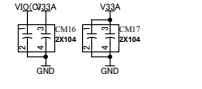
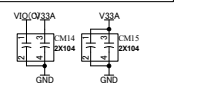
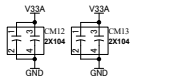
Product information block including part number ACM203R2-SCH-B5.pdf, manufacturer Altera Cyclone III F484 FPGA board, document number ACM-203, and date 30-Jul-2020.



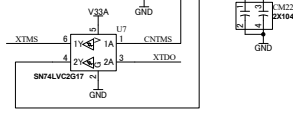
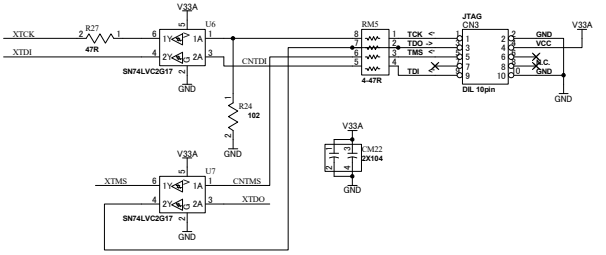
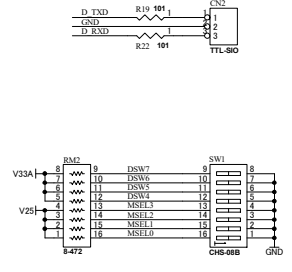
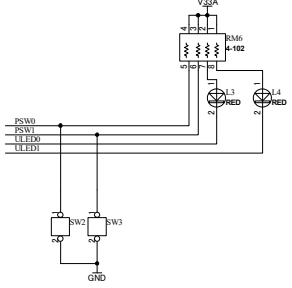
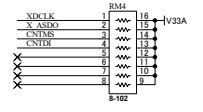
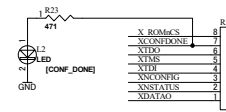
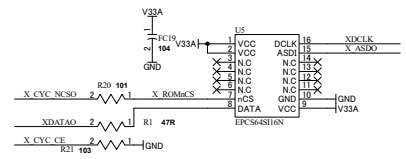
V12	V12
V12D	V12D
V25	V25
V33A	V33A
W0(B)	VIR(B)
W0(C)	VIR(C)
VIO(C)	GND
GND	GND



These pins are connected to VCCIO. You need to set them as INPUT.



BANK Group-A



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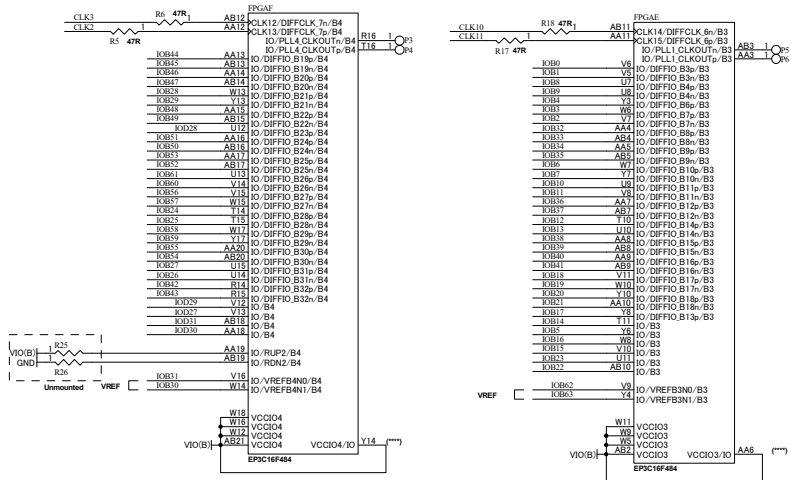


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	Altera Cyclone III F484 FPGA board
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VIO(B) VIO(B)
VIO(C) VIO(C)
GND GND

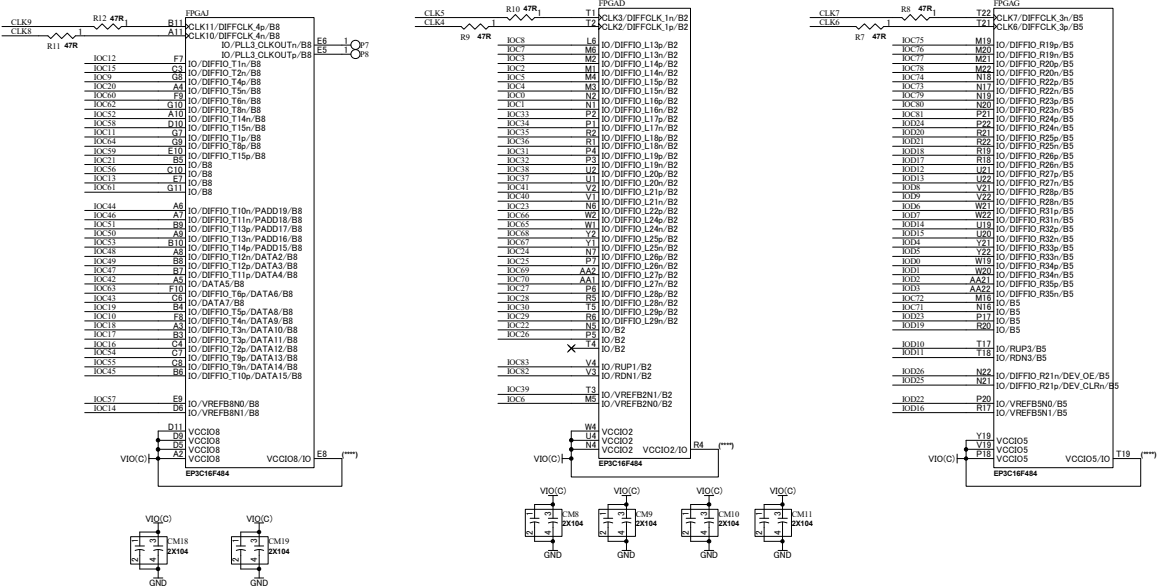
IOB0_63	IOB0_63
IOB0_64	IOB0_64
IOB0_65	IOB0_65
IOB0_66	IOB0_66
IOB0_67	IOB0_67
IOB0_68	IOB0_68
IOB0_69	IOB0_69
IOB0_70	IOB0_70
IOB0_71	IOB0_71
IOB0_72	IOB0_72
IOB0_73	IOB0_73
IOB0_74	IOB0_74
IOB0_75	IOB0_75
IOB0_76	IOB0_76
IOB0_77	IOB0_77
IOB0_78	IOB0_78
IOB0_79	IOB0_79
IOB0_80	IOB0_80
IOB0_81	IOB0_81
IOB0_82	IOB0_82
IOB0_83	IOB0_83
IOB0_84	IOB0_84
IOB0_85	IOB0_85
IOB0_86	IOB0_86
IOB0_87	IOB0_87
IOB0_88	IOB0_88
IOB0_89	IOB0_89
IOB0_90	IOB0_90
IOB0_91	IOB0_91
IOB0_92	IOB0_92
IOB0_93	IOB0_93
IOB0_94	IOB0_94
IOB0_95	IOB0_95
IOB0_96	IOB0_96
IOB0_97	IOB0_97
IOB0_98	IOB0_98
IOB0_99	IOB0_99
IOB0_100	IOB0_100



These pins are connected to VCCIO. You need to set them as INFLUT.

BANK Group-B

BANK Group-C



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DSN	TITLE
	Altera Cyclone III F484 FPGA board
DOC. No.	ACM-203
FILE: FPGA2.sch	DATE: 30-Jul-2020 16:33:40 Sheet 3 / 3
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