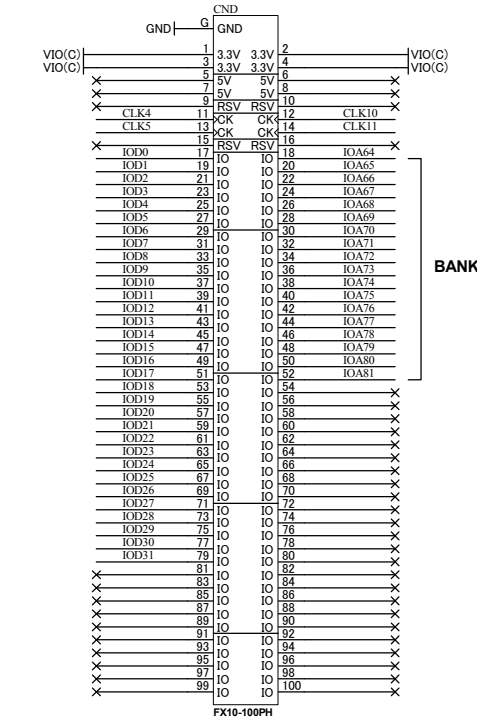
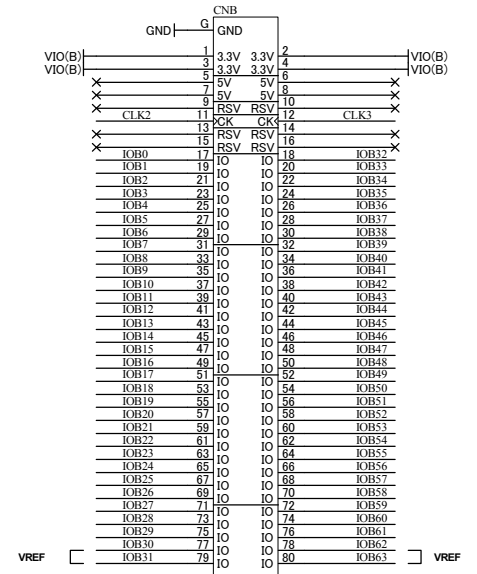
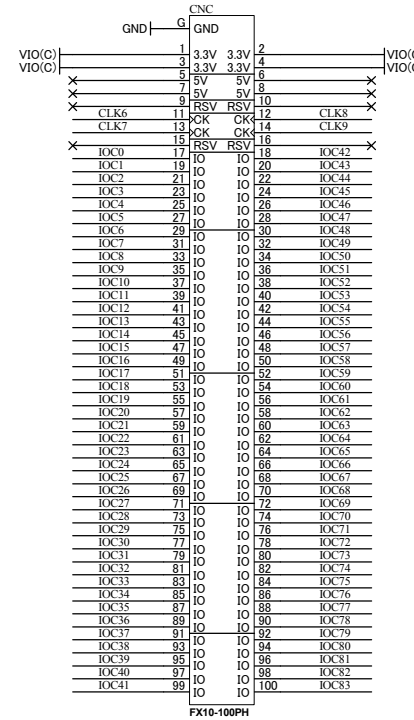
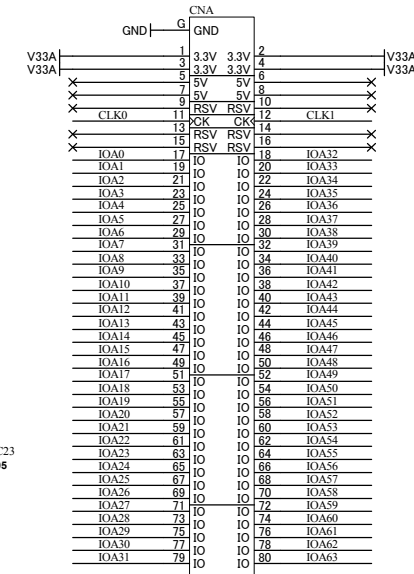
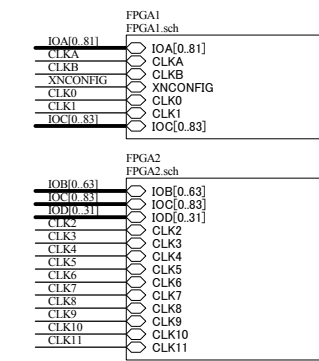
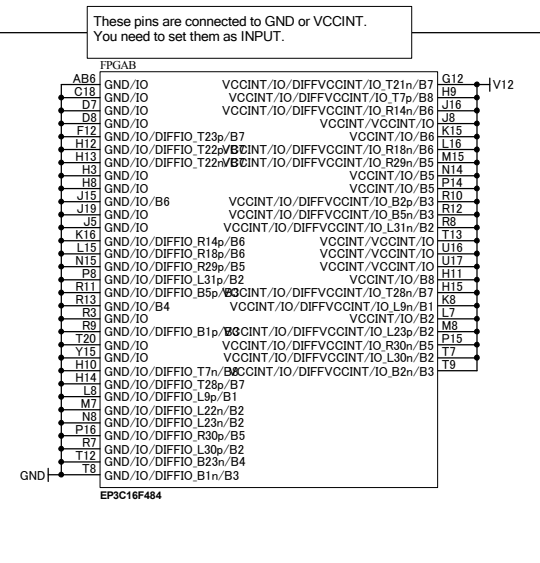
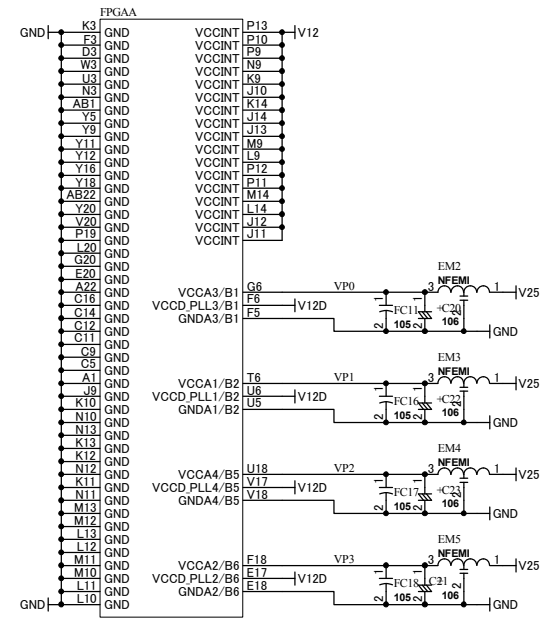
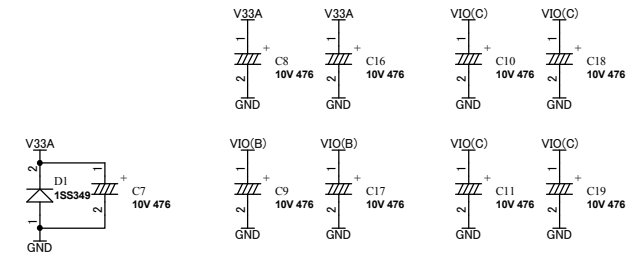
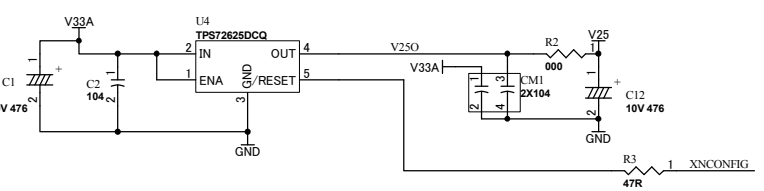
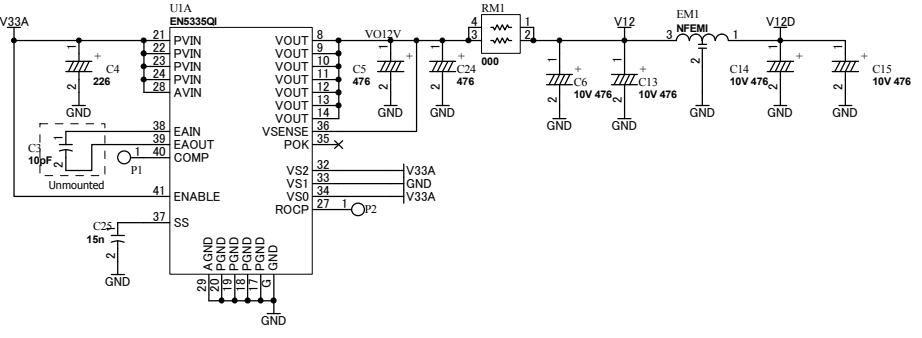
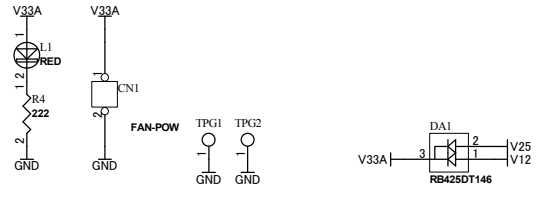
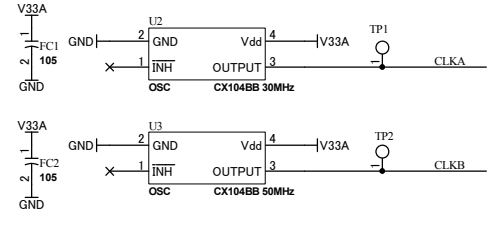


V12 V12D  
 V25 V25D  
 V33A V33A  
 VIO(B) VIO(B)  
 VIO(C) VIO(C)  
 GND GND



BANK Group-A

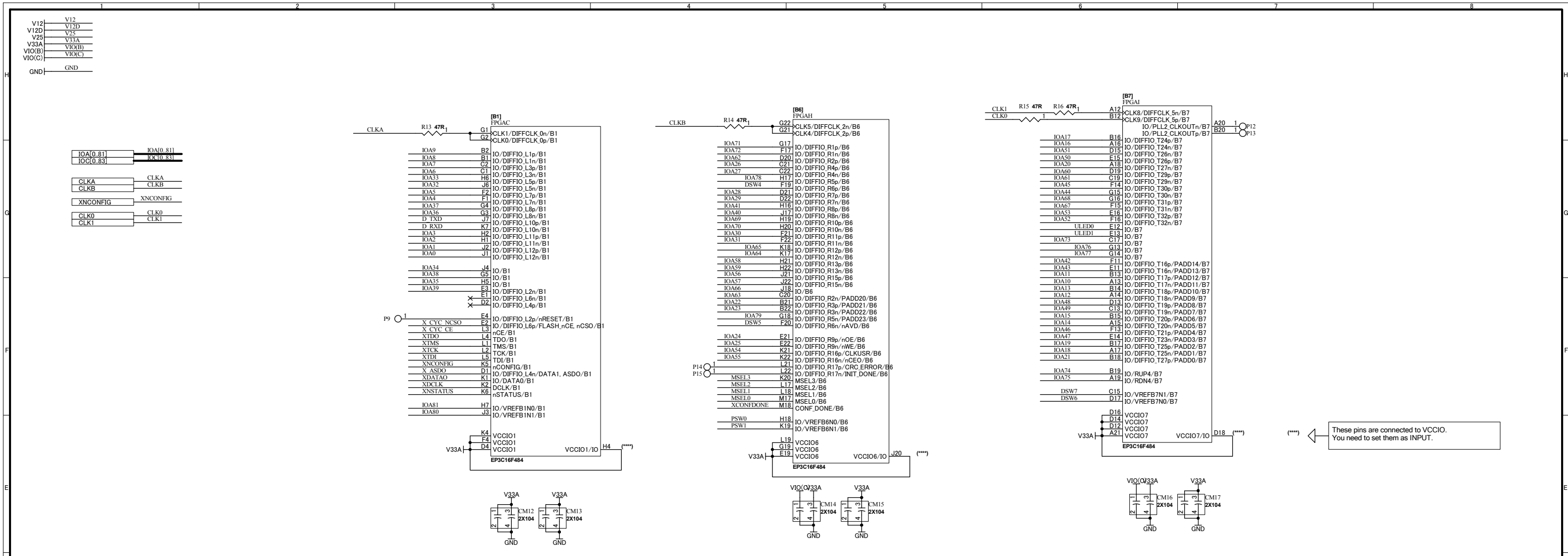


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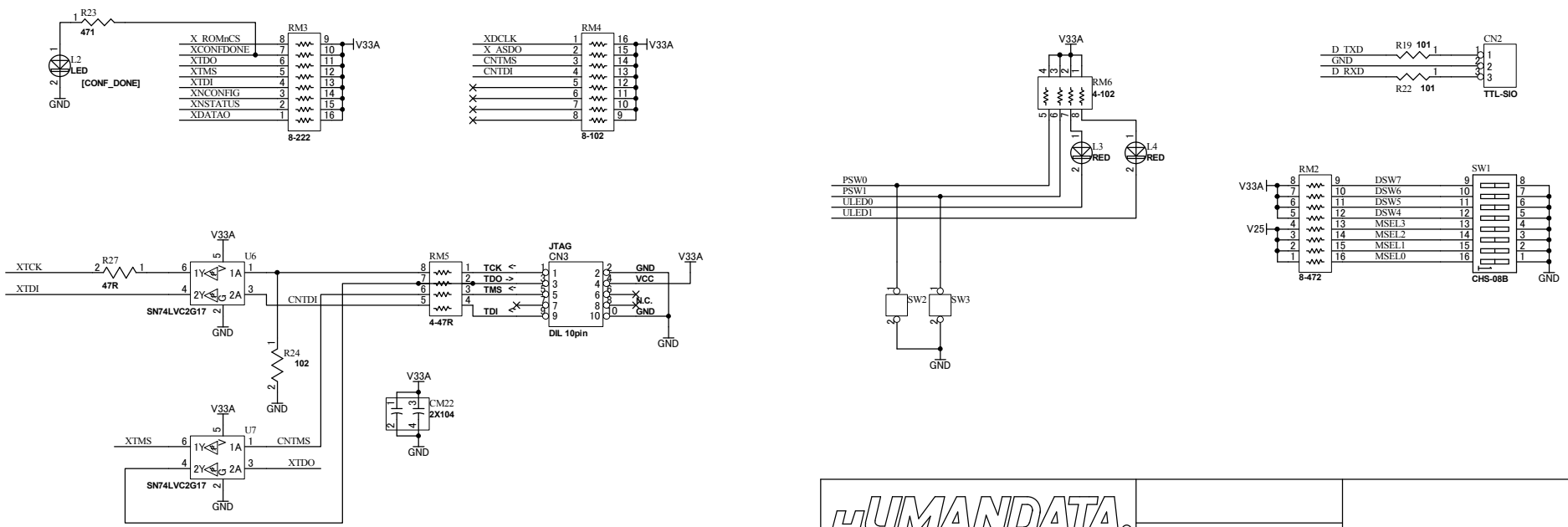
Altera Cyclone III F484 FPGA board

DOC. No. ACM-203

B3



**BANK Group-A**



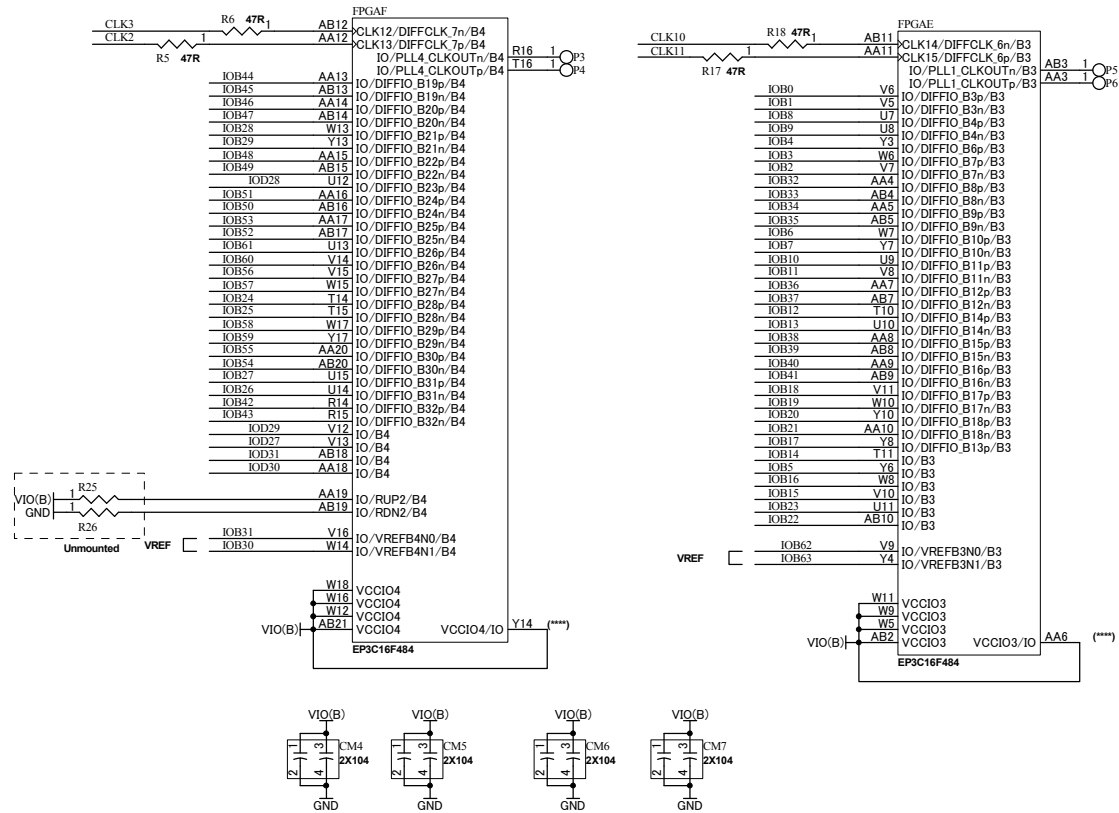
ACM203R2-SCH-B3.pdf

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HuMANDATA LTD. OSAKA JAPAN www.hdl.co.jp/en/(Global) www.hdl.co.jp/(Japan)		Altera Cyclone III F484 FPGA board	
Date:	18-Jul-2012	DOC. No.	ACM-203
	14:04:56	File:	FPGA1.sch
		Sheet	2 of 3
		B3	

VIO(B)  
VIO(C)  
GND

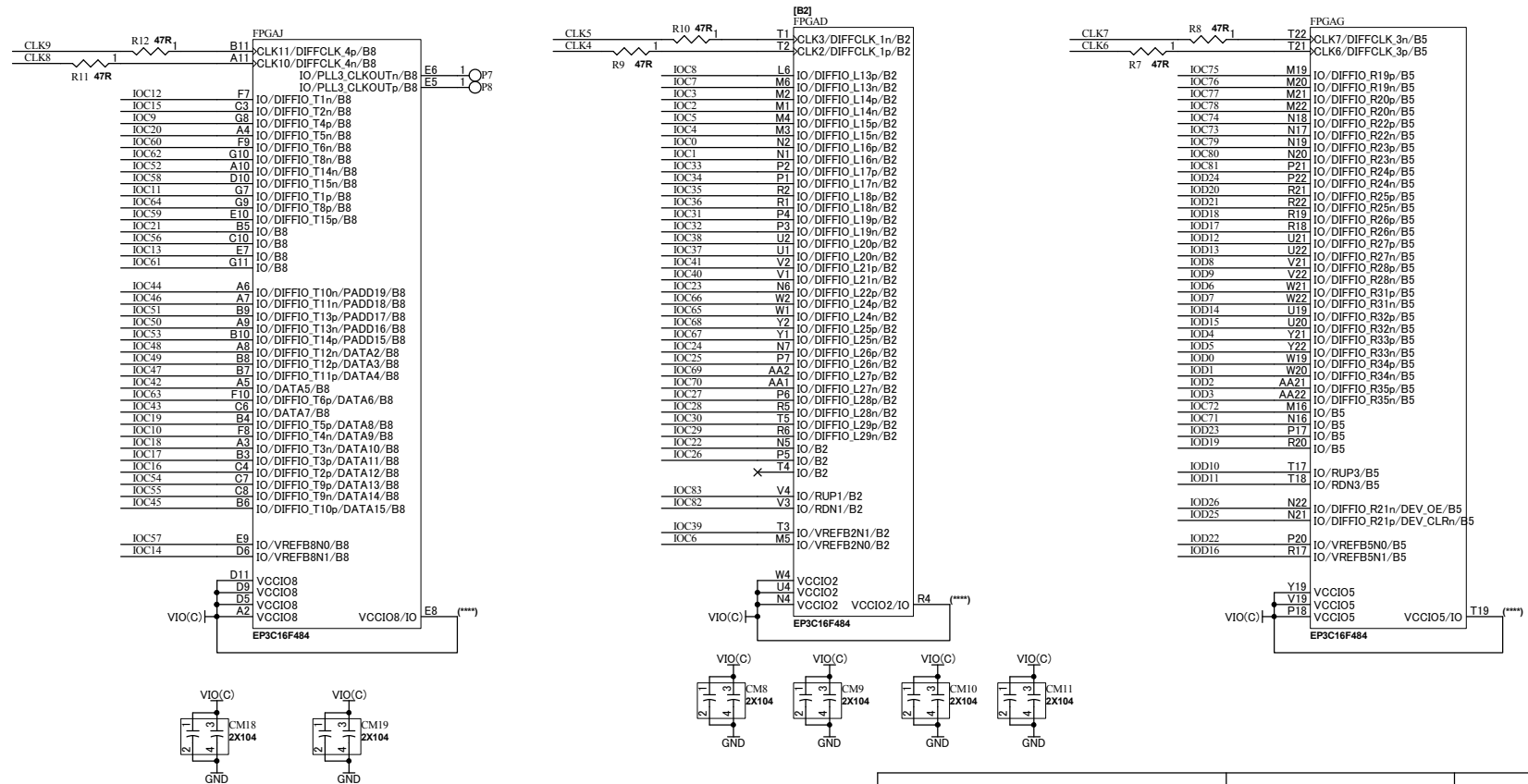
IOB0\_63 IOB0\_63  
IOC0\_83 IOC0\_83  
IOD0\_31 IOD0\_31

CLK2 CLK2  
CLK3 CLK3  
CLK4 CLK4  
CLK5 CLK5  
CLK6 CLK6  
CLK7 CLK7  
CLK8 CLK8  
CLK9 CLK9  
CLK10 CLK10  
CLK11 CLK11



(\*\*\*\*) These pins are connected to VCCIO. You need to set them as INPUT.

**BANK Group-B**  
**BANK Group-C**



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				DOC. No.	ACM-203
Date:	18-Jul-2012	14:04:56	File:	FPGA2.sch	Sheet 3 of 3