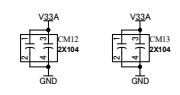
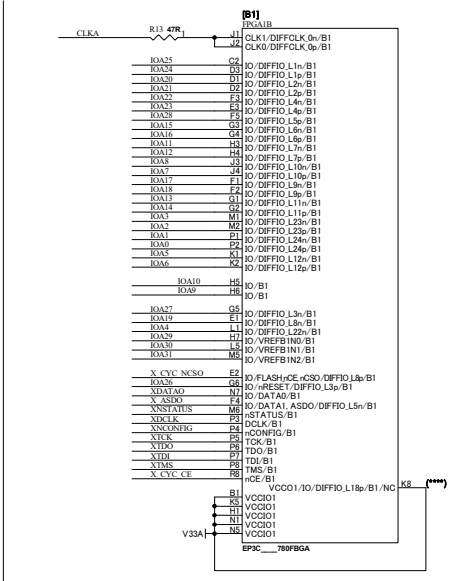


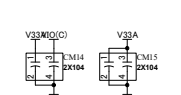
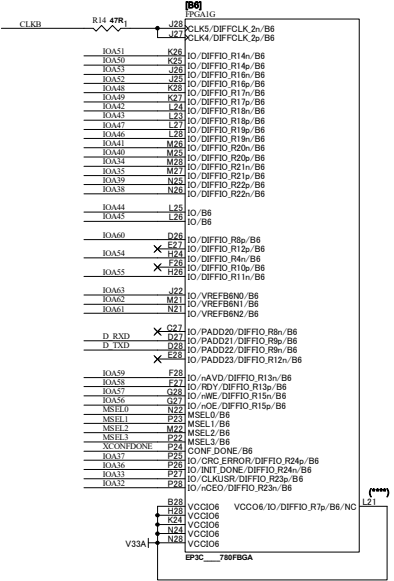


V12	V12
V12A	V12A
V33A	V33A
VIO(B)	VIO(B)
VIO(C)	VIO(C)
VIO(D)	VIO(D)
GND	GND

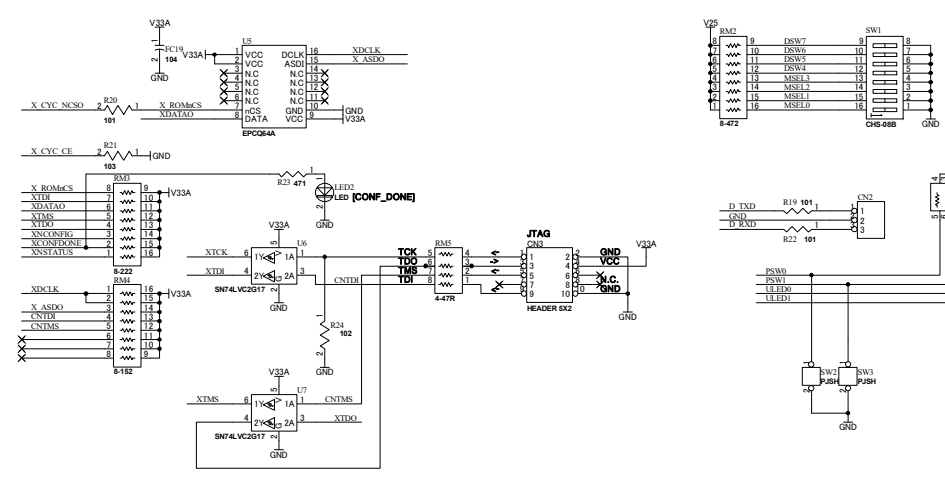
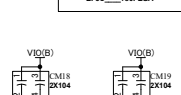
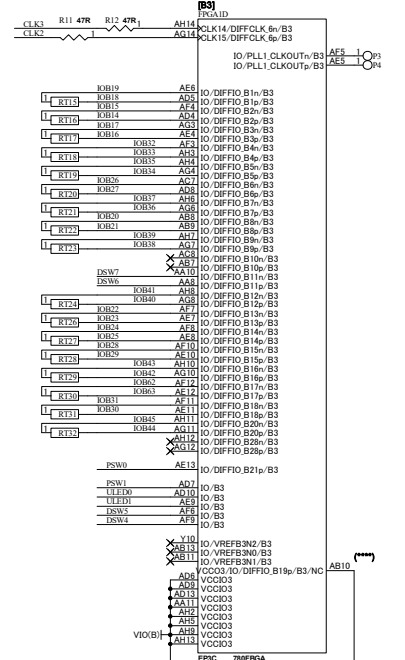
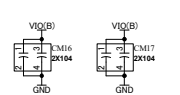
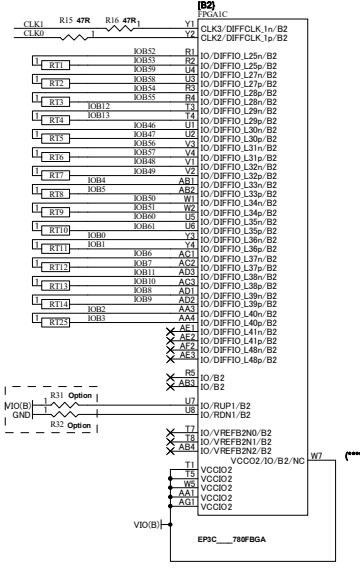
IOA0..53	IOA0..53
IOB0..53	IOB0..53
CLKA	CLKA
CLKB	CLKB
XNCONF0	XNCONF0
CLK0	CLK0
CLK1	CLK1
CLK2	CLK2
CLK3	CLK3



BANK Group A



BANK Group B



These pins are connected to VCCIO. You need to set them as INPUT.

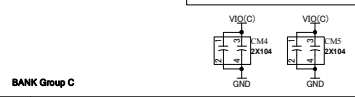
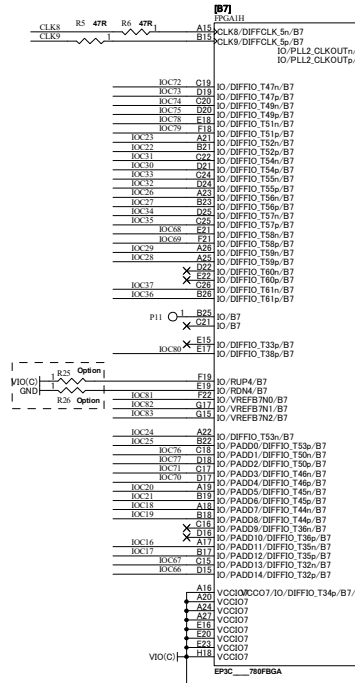


ACM202R3-8CH-A5.pdf	
TITLE Intel CycloneIII F780 FPGA board	
DOC. No.	<b>ACM-202</b>
FILE: FPGA1.ch	DATE: 7-Oct-2020 16:24:03
Sheet	2 / 3

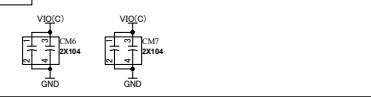
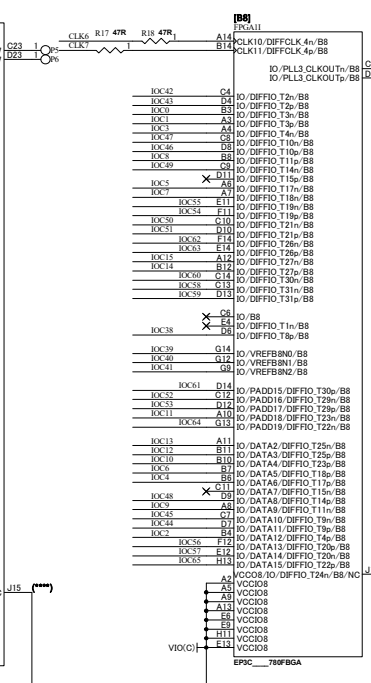
V12 V12  
V12A V12A  
V3A V3A  
V3(B) V3(B)  
V3(C) V3(C)  
V3(D) V3(D)  
GND GND

IO(C)0.83 IO(C)0.83  
IO(D)0.83 IO(D)0.83

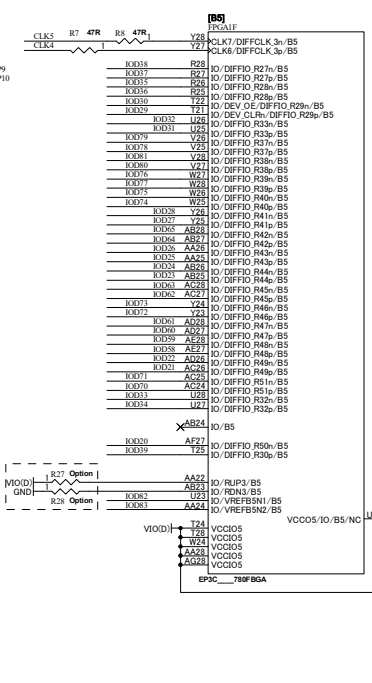
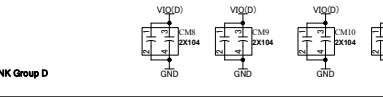
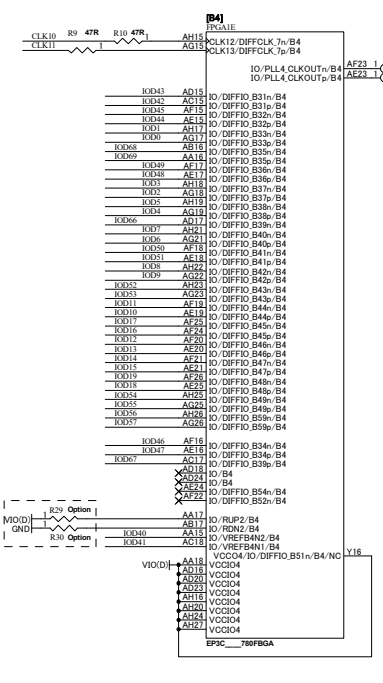
CLK4 CLK4  
CLK5 CLK5  
CLK6 CLK6  
CLK7 CLK7  
CLK8 CLK8  
CLK9 CLK9  
CLK10 CLK10  
CLK11 CLK11



BANK Group C



BANK Group D



IO/CLK0	IO/CLK1	IO/CLK2	IO/CLK3	IO/CLK4	IO/CLK5	IO/CLK6	IO/CLK7	IO/CLK8	IO/CLK9	IO/CLK10	IO/CLK11	IO/CLK12	IO/CLK13	IO/CLK14	IO/CLK15	IO/CLK16	IO/CLK17	IO/CLK18	IO/CLK19	IO/CLK20	IO/CLK21	IO/CLK22	IO/CLK23	IO/CLK24	IO/CLK25	IO/CLK26	IO/CLK27	IO/CLK28	IO/CLK29	IO/CLK30	IO/CLK31	IO/CLK32	IO/CLK33	IO/CLK34	IO/CLK35	IO/CLK36	IO/CLK37	IO/CLK38	IO/CLK39	IO/CLK40	IO/CLK41	IO/CLK42	IO/CLK43	IO/CLK44	IO/CLK45	IO/CLK46	IO/CLK47	IO/CLK48	IO/CLK49	IO/CLK50	IO/CLK51	IO/CLK52	IO/CLK53	IO/CLK54	IO/CLK55	IO/CLK56	IO/CLK57	IO/CLK58	IO/CLK59	IO/CLK60	IO/CLK61	IO/CLK62	IO/CLK63	IO/CLK64	IO/CLK65	IO/CLK66	IO/CLK67	IO/CLK68	IO/CLK69	IO/CLK70	IO/CLK71	IO/CLK72	IO/CLK73	IO/CLK74	IO/CLK75	IO/CLK76	IO/CLK77	IO/CLK78	IO/CLK79	IO/CLK80	IO/CLK81	IO/CLK82	IO/CLK83	IO/CLK84	IO/CLK85	IO/CLK86	IO/CLK87	IO/CLK88	IO/CLK89	IO/CLK90	IO/CLK91	IO/CLK92	IO/CLK93	IO/CLK94	IO/CLK95	IO/CLK96	IO/CLK97	IO/CLK98	IO/CLK99	IO/CLK100
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(\*\*\*) These pins are connected to VCCIO. You need to set them as INPUT.

