

These pins are connected to VCCINT.  
You need to set them as INPUT.

These pins are connected to GND.  
You need to set them as INPUT.

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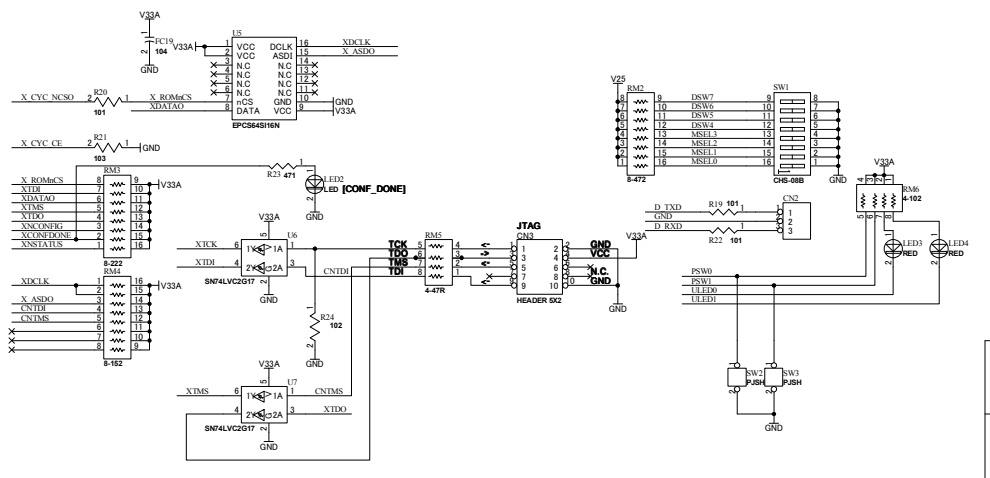
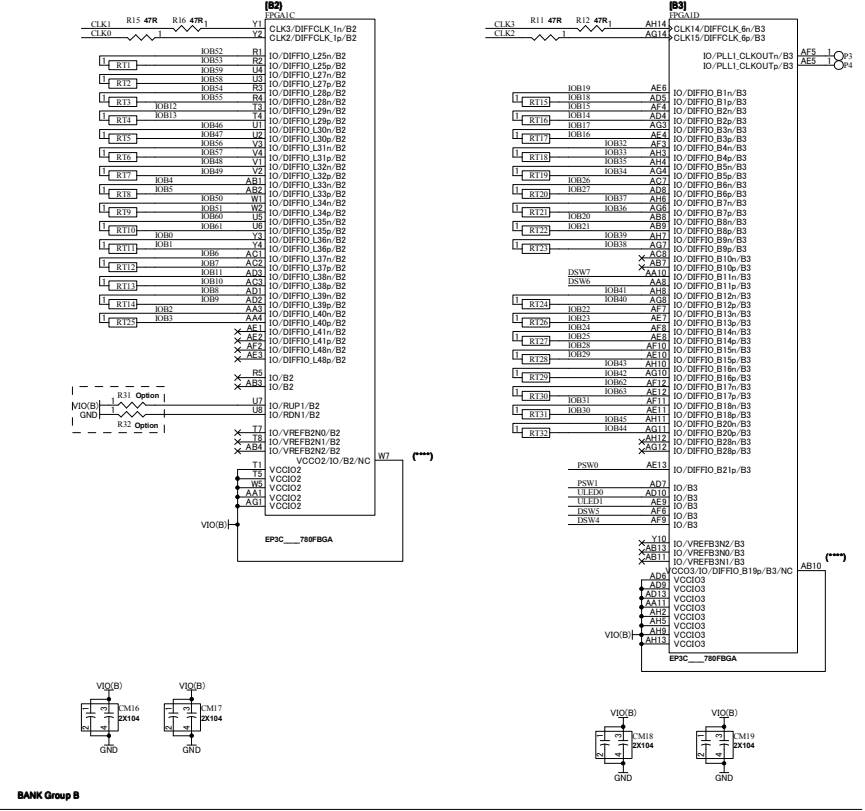
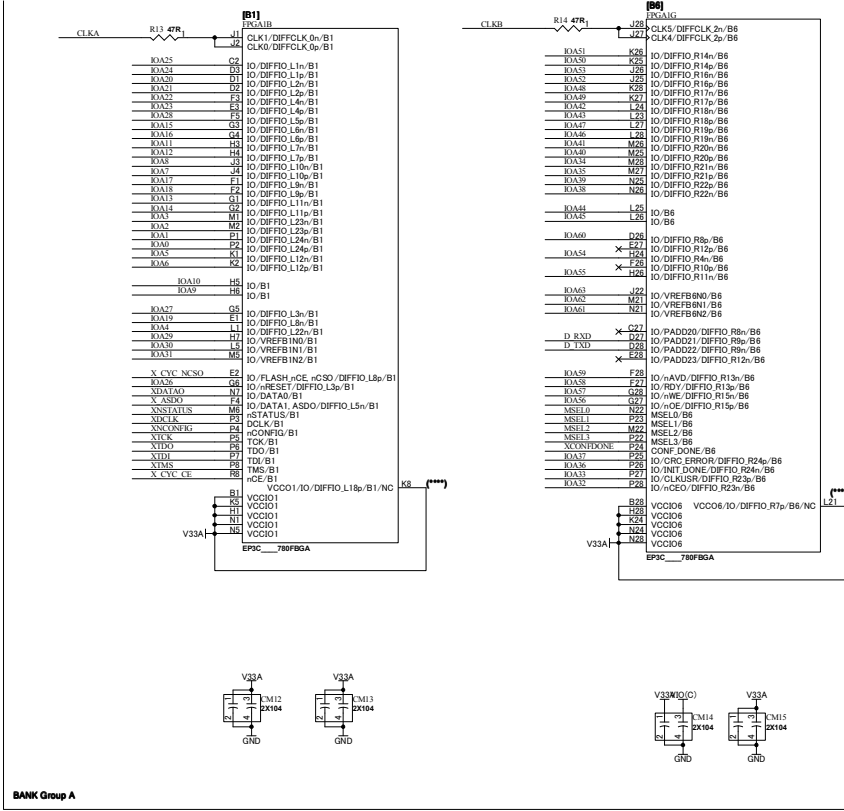
Altera CycloneIII F780 FPGA board

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V12	V12
V12A	V12A
V33A	V33A
VIO(B)	VIO(B)
VIO(C)	VIO(C)
VIO(D)	VIO(D)
GND	GND

[DA0_63]	DA0_63
[DB0_63]	DB0_63
CLKA	CLKA
CLKB	CLKB
NNCONF0	NNCONF0
CLK0	CLK0
CLK1	CLK1
CLK2	CLK2
CLK3	CLK3



These pins are connected to VCCIO. You need to set them as INPUT.

ACM202R2-SCH-A4.pdf

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V12 V12  
V12A V12A  
V5A V5A  
VIO(B) VIO(B)  
VIO(C) VIO(C)  
VIO(D) VIO(D)  
GND GND

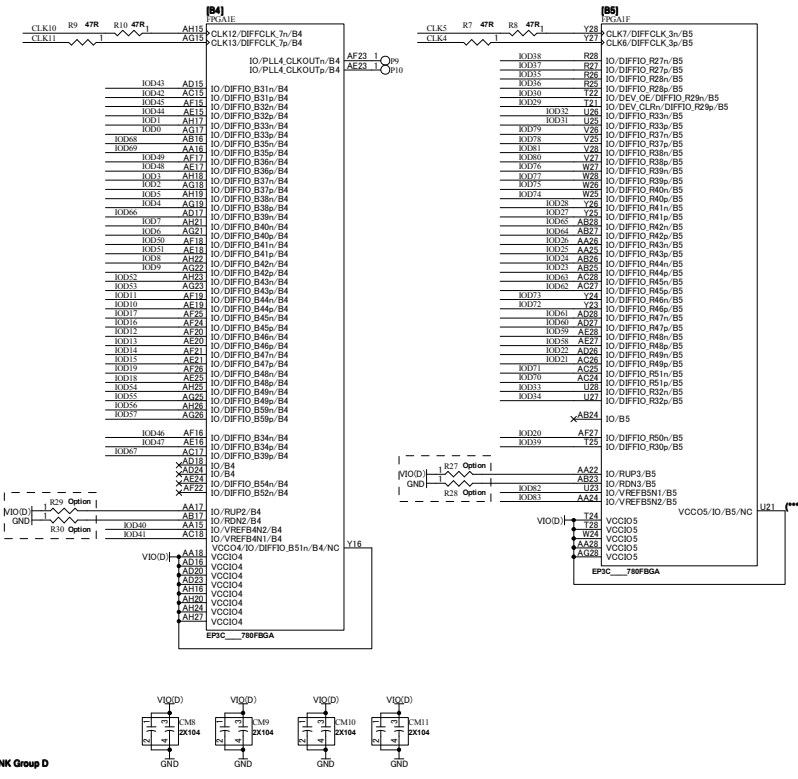
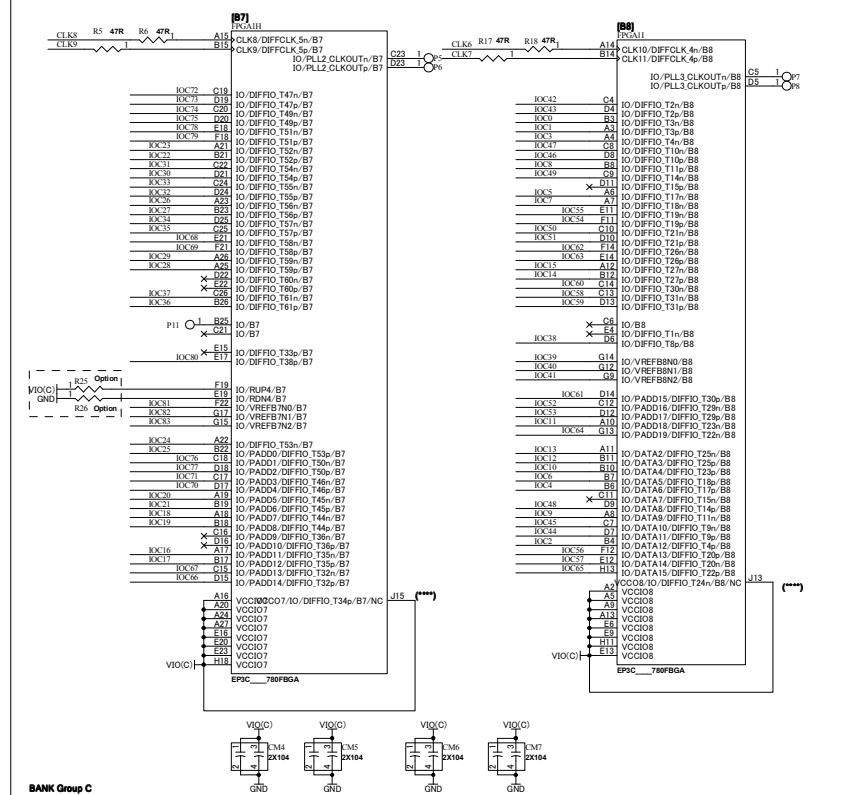


Table of pin connections for BANK Group C and D, showing pin numbers and their functions (e.g., IO/DIFCLK, IO/PADD, IO/VREF).

Table of pin connections for BANK Group E and F, showing pin numbers and their functions (e.g., IO/DIFCLK, IO/PADD, IO/VREF).

(\*\*\*) These pins are connected to VCCIO. You need to set them as INPUT.

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Altera CycloneIII F780 FPGA board

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