

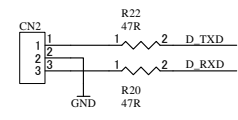
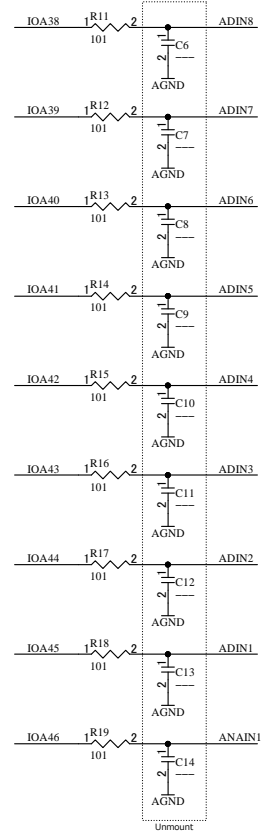
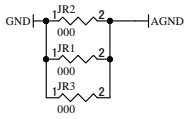
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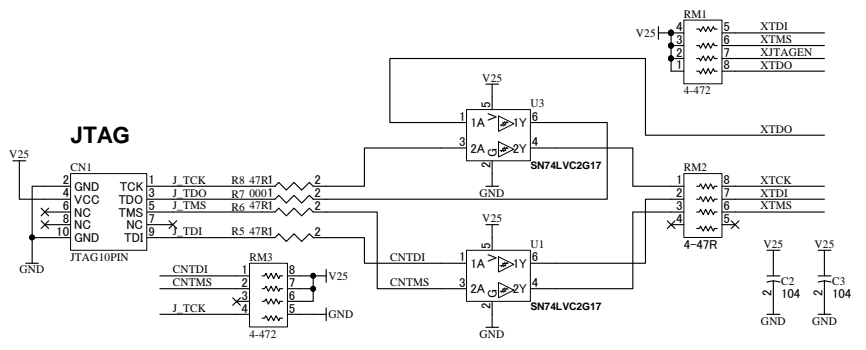
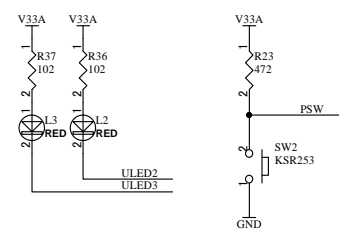
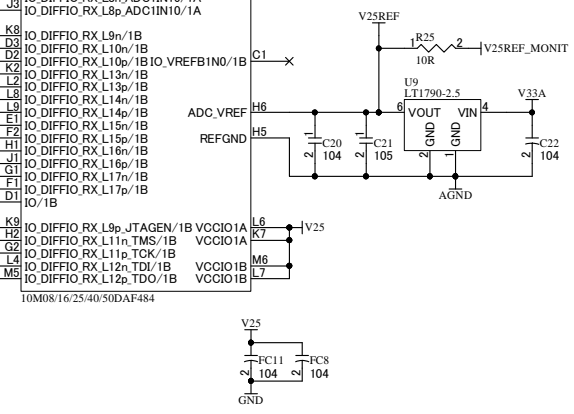
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V33A V33A
 VIO(B) VIO(B)
 V25 V25
 V12ORG V12ORG
 GND GND

IOA10.631



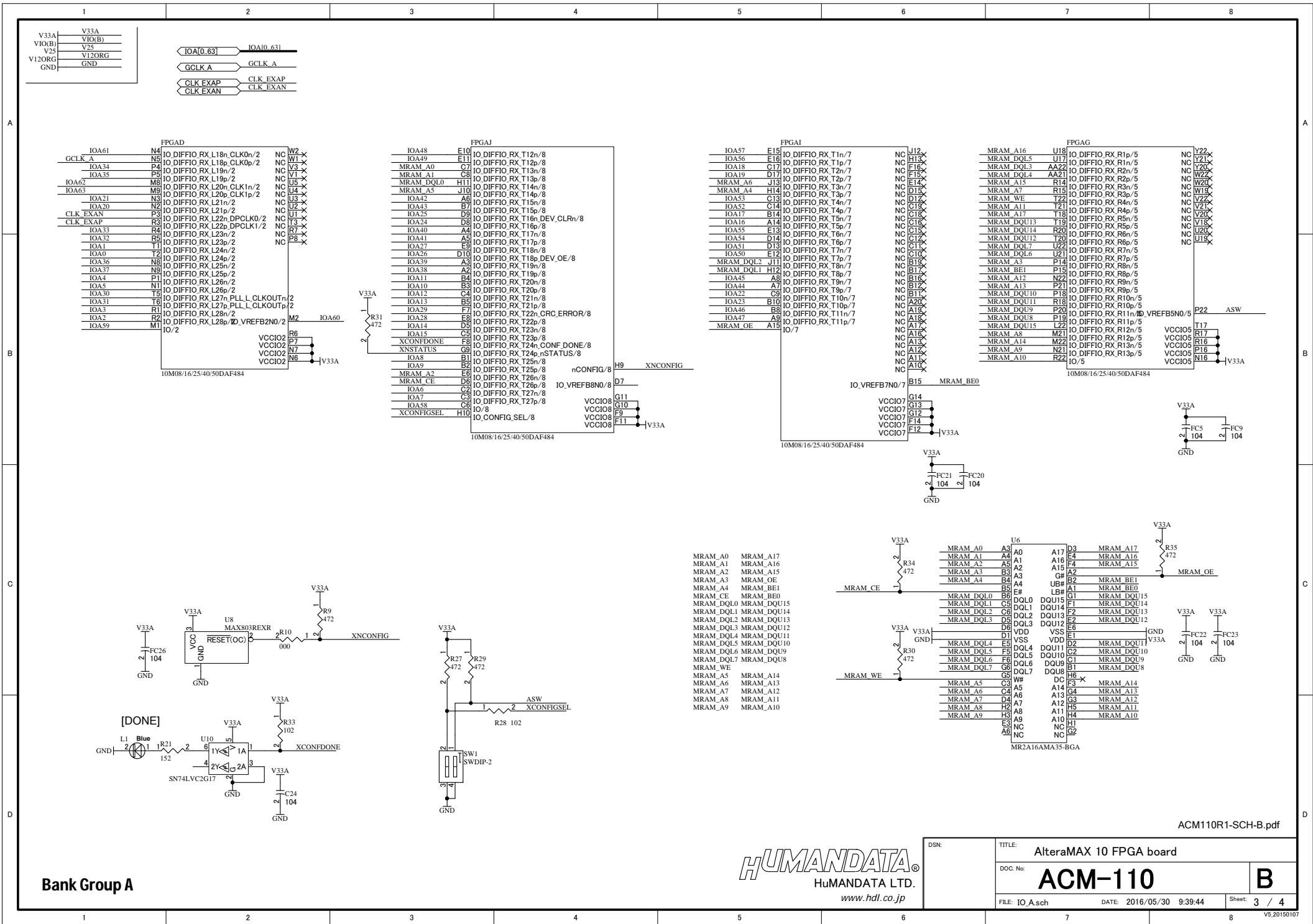
Signal	FPGA Pin	IO Pin	IO Pin
ANAIN1	G5	ANAIN1	NC
ADIN1	F5	NC	ANAIN2
ADIN2	F4	IO DIFFIO_RX L1n, ADCI1N1/1A	NC
	E4	IO DIFFIO_RX L1p, ADCI1N2/1A	NC
	E3	IO DIFFIO_RX L2n, ADCI1N9/1A	NC
ADIN3	E8	IO DIFFIO_RX L2p, ADCI1N16/1A	
ADIN4	J9	IO DIFFIO_RX L3n, ADCI1N3/1A	
	G4	IO DIFFIO_RX L3p, ADCI1N4/1A	
ADIN5	F3	IO DIFFIO_RX L4n, ADCI1N11/1A	
ADIN6	H4	IO DIFFIO_RX L4p, ADCI1N12/1A	
	H3	IO DIFFIO_RX L5n, ADCI1N5/1A	
	H4	IO DIFFIO_RX L5p, ADCI1N6/1A	
ADIN7	G3	IO DIFFIO_RX L8n, ADCI1N13/1A	
ADIN8	K5	IO DIFFIO_RX L7n, ADCI1N7/1A	
	K4	IO DIFFIO_RX L7p, ADCI1N8/1A	
	J3	IO DIFFIO_RX L8n, ADCI1N15/1A	
	J3	IO DIFFIO_RX L8p, ADCI1N10/1A	
D_TXD	K8	IO DIFFIO_RX L9n/1B	
D_RXD	D9	IO DIFFIO_RX L10n/1B	
	K2	IO DIFFIO_RX L10p/1B IO_VREFB1N0/1B	
	L2	IO DIFFIO_RX L13n/1B	
	L8	IO DIFFIO_RX L14n/1B	
	L9	IO DIFFIO_RX L14p/1B	
	E1	IO DIFFIO_RX L13n/1B	
	E2	IO DIFFIO_RX L15n/1B	
	H1	IO DIFFIO_RX L16n/1B	
	J1	IO DIFFIO_RX L16p/1B	
PSW	G1	IO DIFFIO_RX L17n/1B	
ULED2	F1	IO DIFFIO_RX L17p/1B	
ULED3	D1	IO/1B	
XJTAGEN	K9	IO DIFFIO_RX L9p, JTAGEN/1B VCCIO1A	L6
XTMS	H2	IO DIFFIO_RX L11n, TMS/1B VCCIO1A	K7
XTCK	G2	IO DIFFIO_RX L11p, TCK/1B	M6
XTDI	L4	IO DIFFIO_RX L12n, TDI/1B VCCIO1B	L7
XTDO	M5	IO DIFFIO_RX L12p, TDO/1B VCCIO1B	



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HUMAN DATA
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Bank Group A

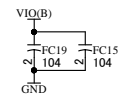
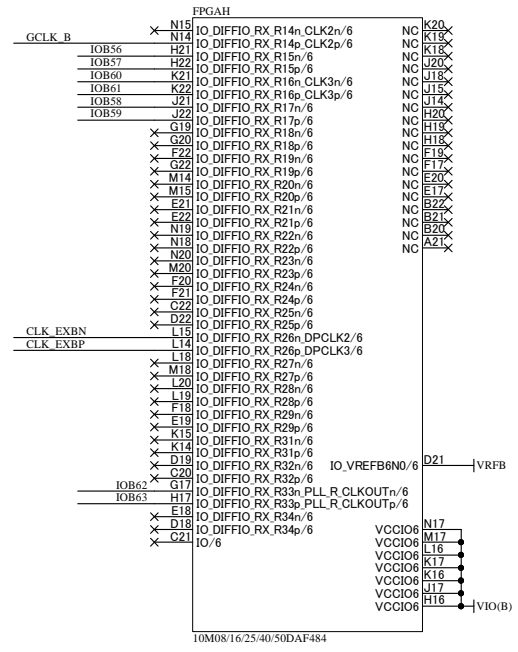
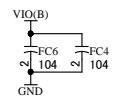
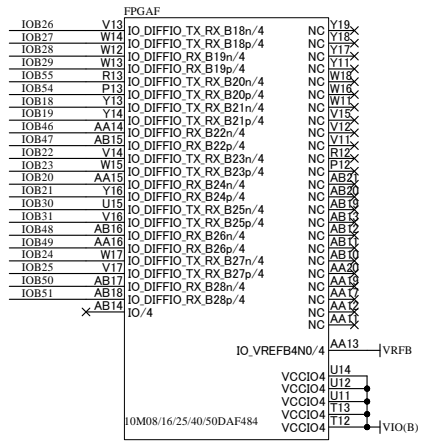
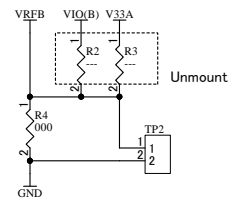
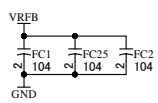
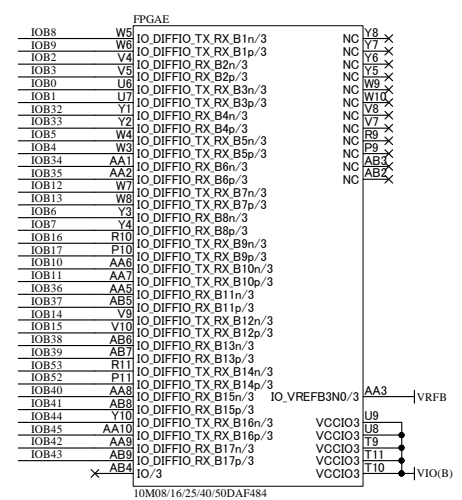
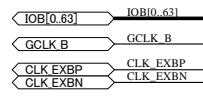
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V5.20150107

V33A
VIO(B)
V25
V12ORG
GND



Bank Group B



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