

Bank Group A

Bank Group B



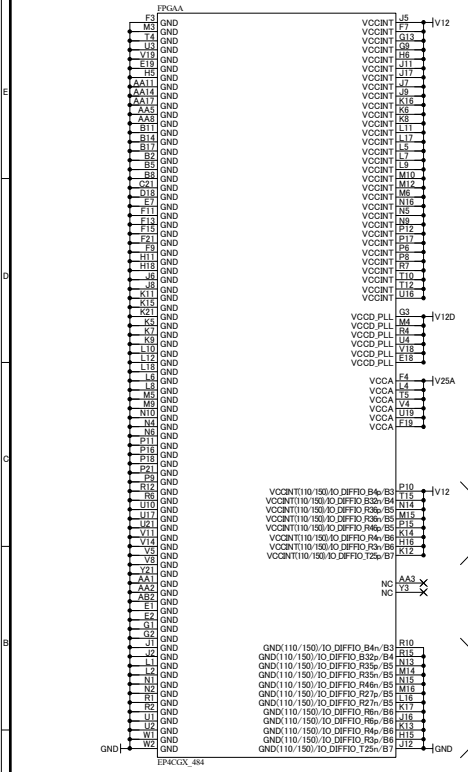
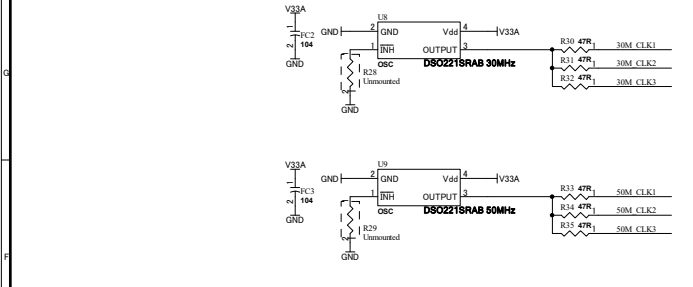
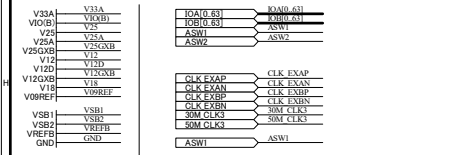
ACM108R-8CH-C3.pdf

ALTERA Cyclone IV GX F484 FPGA board

DOC No: **ACM-108**

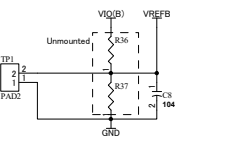
FILE: ACM108C.sch DATE: 23-Mar-2020 10:27:49 Sheet: 1 / 3

C3

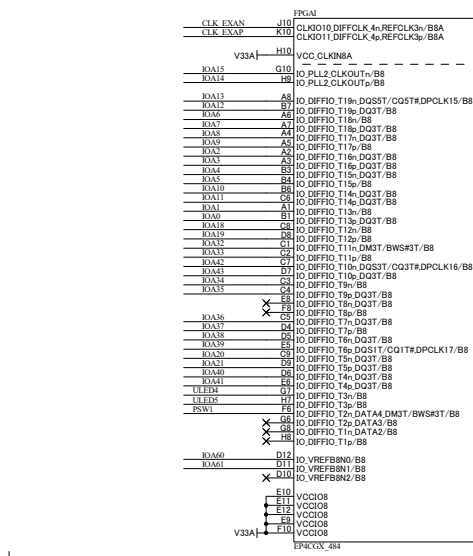


These pins are connected to VCCINT. You need to set them as INPUT.

These pins are connected to GND. You need to set them as INPUT.



RIGHT EDGE [BANK 5/6] for Bank Group B



TOP EDGE [BANK 7/8] for Bank Group A



| IO | DIFFCLK | DM3R/BWS5R/B5 |
|-------|----------------|---------------|
| IOB00 | DIFFCLK_0n/B5 | DM3R/BWS5R/B5 |
| IOB01 | DIFFCLK_1n/B5 | DM3R/BWS5R/B5 |
| IOB02 | DIFFCLK_2n/B5 | DM3R/BWS5R/B5 |
| IOB03 | DIFFCLK_3n/B5 | DM3R/BWS5R/B5 |
| IOB04 | DIFFCLK_4n/B5 | DM3R/BWS5R/B5 |
| IOB05 | DIFFCLK_5n/B5 | DM3R/BWS5R/B5 |
| IOB06 | DIFFCLK_6n/B5 | DM3R/BWS5R/B5 |
| IOB07 | DIFFCLK_7n/B5 | DM3R/BWS5R/B5 |
| IOB08 | DIFFCLK_8n/B5 | DM3R/BWS5R/B5 |
| IOB09 | DIFFCLK_9n/B5 | DM3R/BWS5R/B5 |
| IOB10 | DIFFCLK_10n/B5 | DM3R/BWS5R/B5 |
| IOB11 | DIFFCLK_11n/B5 | DM3R/BWS5R/B5 |
| IOB12 | DIFFCLK_12n/B5 | DM3R/BWS5R/B5 |
| IOB13 | DIFFCLK_13n/B5 | DM3R/BWS5R/B5 |
| IOB14 | DIFFCLK_14n/B5 | DM3R/BWS5R/B5 |
| IOB15 | DIFFCLK_15n/B5 | DM3R/BWS5R/B5 |
| IOB16 | DIFFCLK_16n/B5 | DM3R/BWS5R/B5 |
| IOB17 | DIFFCLK_17n/B5 | DM3R/BWS5R/B5 |
| IOB18 | DIFFCLK_18n/B5 | DM3R/BWS5R/B5 |
| IOB19 | DIFFCLK_19n/B5 | DM3R/BWS5R/B5 |
| IOB20 | DIFFCLK_20n/B5 | DM3R/BWS5R/B5 |
| IOB21 | DIFFCLK_21n/B5 | DM3R/BWS5R/B5 |
| IOB22 | DIFFCLK_22n/B5 | DM3R/BWS5R/B5 |
| IOB23 | DIFFCLK_23n/B5 | DM3R/BWS5R/B5 |
| IOB24 | DIFFCLK_24n/B5 | DM3R/BWS5R/B5 |
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| IOB28 | DIFFCLK_28n/B5 | DM3R/BWS5R/B5 |
| IOB29 | DIFFCLK_29n/B5 | DM3R/BWS5R/B5 |
| IOB30 | DIFFCLK_30n/B5 | DM3R/BWS5R/B5 |
| IOB31 | DIFFCLK_31n/B5 | DM3R/BWS5R/B5 |
| IOB32 | DIFFCLK_32n/B5 | DM3R/BWS5R/B5 |
| IOB33 | DIFFCLK_33n/B5 | DM3R/BWS5R/B5 |
| IOB34 | DIFFCLK_34n/B5 | DM3R/BWS5R/B5 |
| IOB35 | DIFFCLK_35n/B5 | DM3R/BWS5R/B5 |
| IOB36 | DIFFCLK_36n/B5 | DM3R/BWS5R/B5 |
| IOB37 | DIFFCLK_37n/B5 | DM3R/BWS5R/B5 |
| IOB38 | DIFFCLK_38n/B5 | DM3R/BWS5R/B5 |
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| IOB40 | DIFFCLK_40n/B5 | DM3R/BWS5R/B5 |
| IOB41 | DIFFCLK_41n/B5 | DM3R/BWS5R/B5 |
| IOB42 | DIFFCLK_42n/B5 | DM3R/BWS5R/B5 |
| IOB43 | DIFFCLK_43n/B5 | DM3R/BWS5R/B5 |
| IOB44 | DIFFCLK_44n/B5 | DM3R/BWS5R/B5 |
| IOB45 | DIFFCLK_45n/B5 | DM3R/BWS5R/B5 |
| IOB46 | DIFFCLK_46n/B5 | DM3R/BWS5R/B5 |
| IOB47 | DIFFCLK_47n/B5 | DM3R/BWS5R/B5 |
| IOB48 | DIFFCLK_48n/B5 | DM3R/BWS5R/B5 |
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| IOB50 | DIFFCLK_50n/B5 | DM3R/BWS5R/B5 |
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| IOB60 | DIFFCLK_60n/B5 | DM3R/BWS5R/B5 |
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| IOB80 | DIFFCLK_80n/B5 | DM3R/BWS5R/B5 |
| IOB81 | DIFFCLK_81n/B5 | DM3R/BWS5R/B5 |
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| IOB98 | DIFFCLK_98n/B5 | DM3R/BWS5R/B5 |
| IOB99 | DIFFCLK_99n/B5 | DM3R/BWS5R/B5 |

| IO | DIFFCLK | DM3R/BWS5R/B5 |
|--------|-----------------|---------------|
| IOB100 | DIFFCLK_100n/B5 | DM3R/BWS5R/B5 |
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| IOB197 | DIFFCLK_197n/B5 | DM3R/BWS5R/B5 |
| IOB198 | DIFFCLK_198n/B5 | DM3R/BWS5R/B5 |
| IOB199 | DIFFCLK_199n/B5 | DM3R/BWS5R/B5 |

ACM108A-SCH-C3.pdf

DRAWING TITLE

ALTERA Cyclone IV GX F484 FPGA board

DOC No: **ACM-108**

FILE: FPGA1.sch DATE: 23-Mar-2020 10:27:50 Sheet: 2 / 3

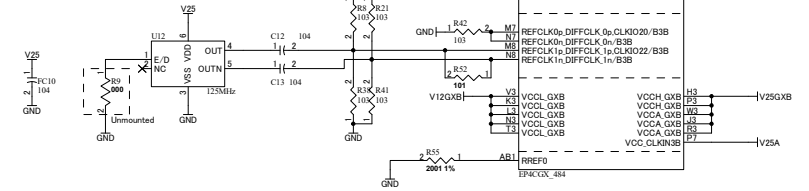
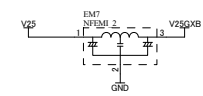
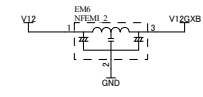
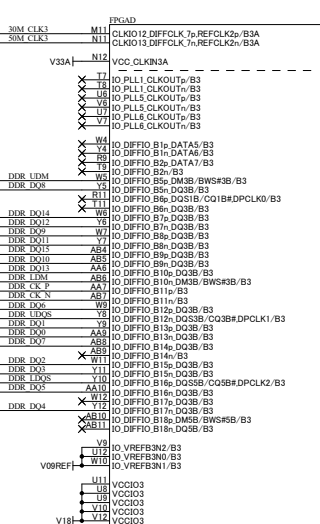
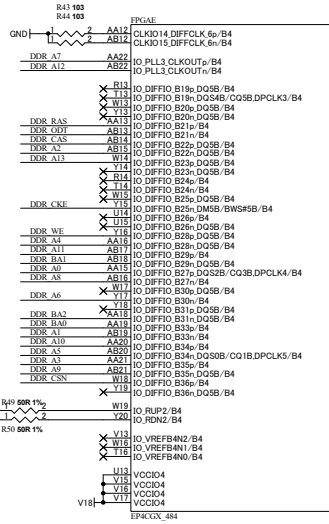
C3

932192102

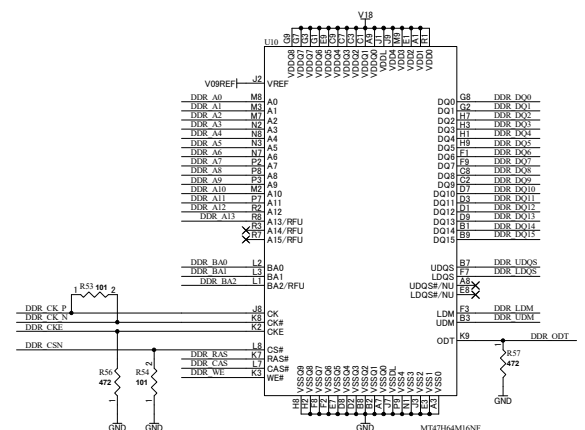
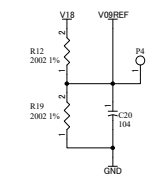


| | |
|--------|--------|
| V33A | V33A |
| V0[B] | V0[B] |
| V25 | V25 |
| V25A | V25A |
| V25QXB | V25QXB |
| V12 | V12 |
| V12D | V12D |
| V12QXB | V12QXB |
| V18 | V18 |
| V18REF | V18REF |
| VSB1 | VSB1 |
| VSB2 | VSB2 |
| GND | GND |

| | |
|----------|----------|
| 30M_CLK3 | 30M_CLK3 |
| 30M_CLK3 | 30M_CLK3 |
| GXB_TX3P | GXB_TX3P |
| GXB_TX3N | GXB_TX3N |
| GXB_RX3P | GXB_RX3P |
| GXB_RX3N | GXB_RX3N |
| GXB_TX0P | GXB_TX0P |
| GXB_TX0N | GXB_TX0N |
| GXB_RX0P | GXB_RX0P |
| GXB_RX0N | GXB_RX0N |
| GND | GND |



LEFT EDGE for HI-SPEED TRASCEIVER



BOTTOM EDGE [BANK 3/4] for DDR2 SDRAM



| | |
|---|--|
| ACM108R-8CH-C3.pdf | |
| TITLE ALTERA Cyclone IV GX F484 FPGA board | |
| DOC No ACM-108 | C3 |
| FILE: FPGA2.sch | DATE: 23-Mar-2020 10:27:51 Sheet 3 / 3 |