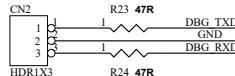


Bank Group A(3.3V)

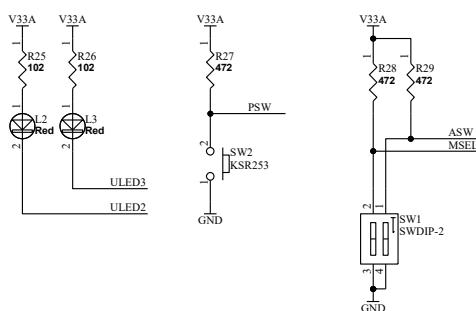
A



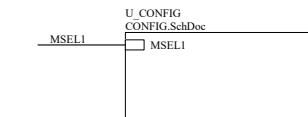
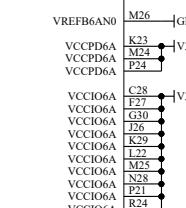
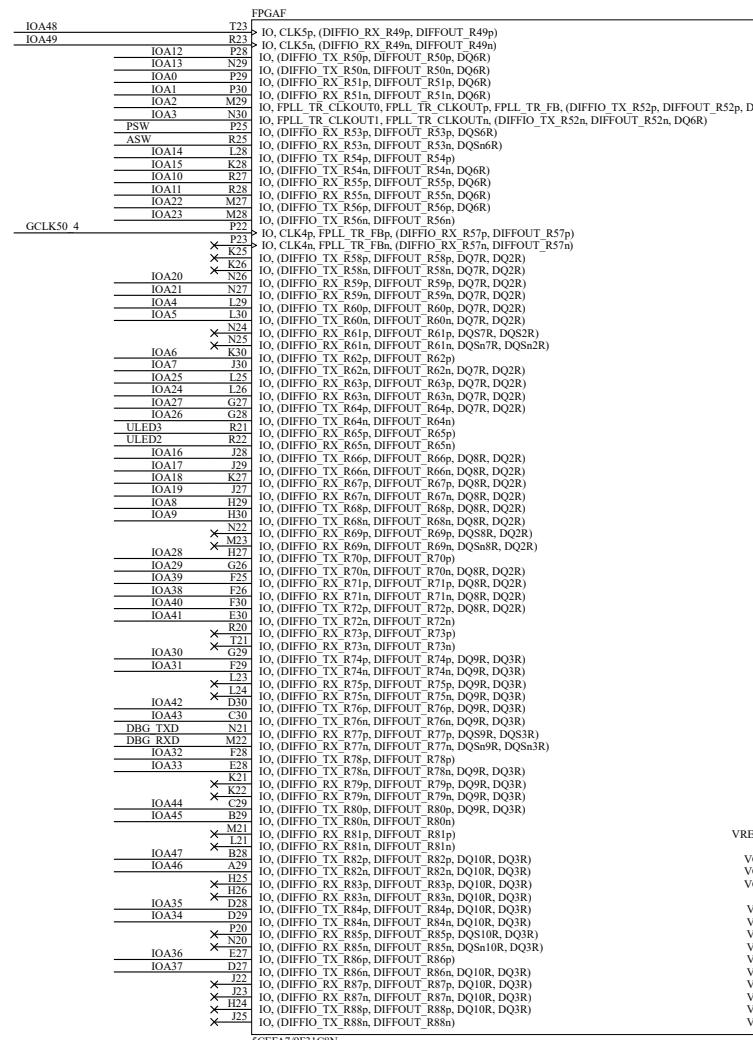
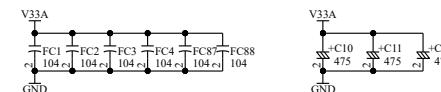
B



C



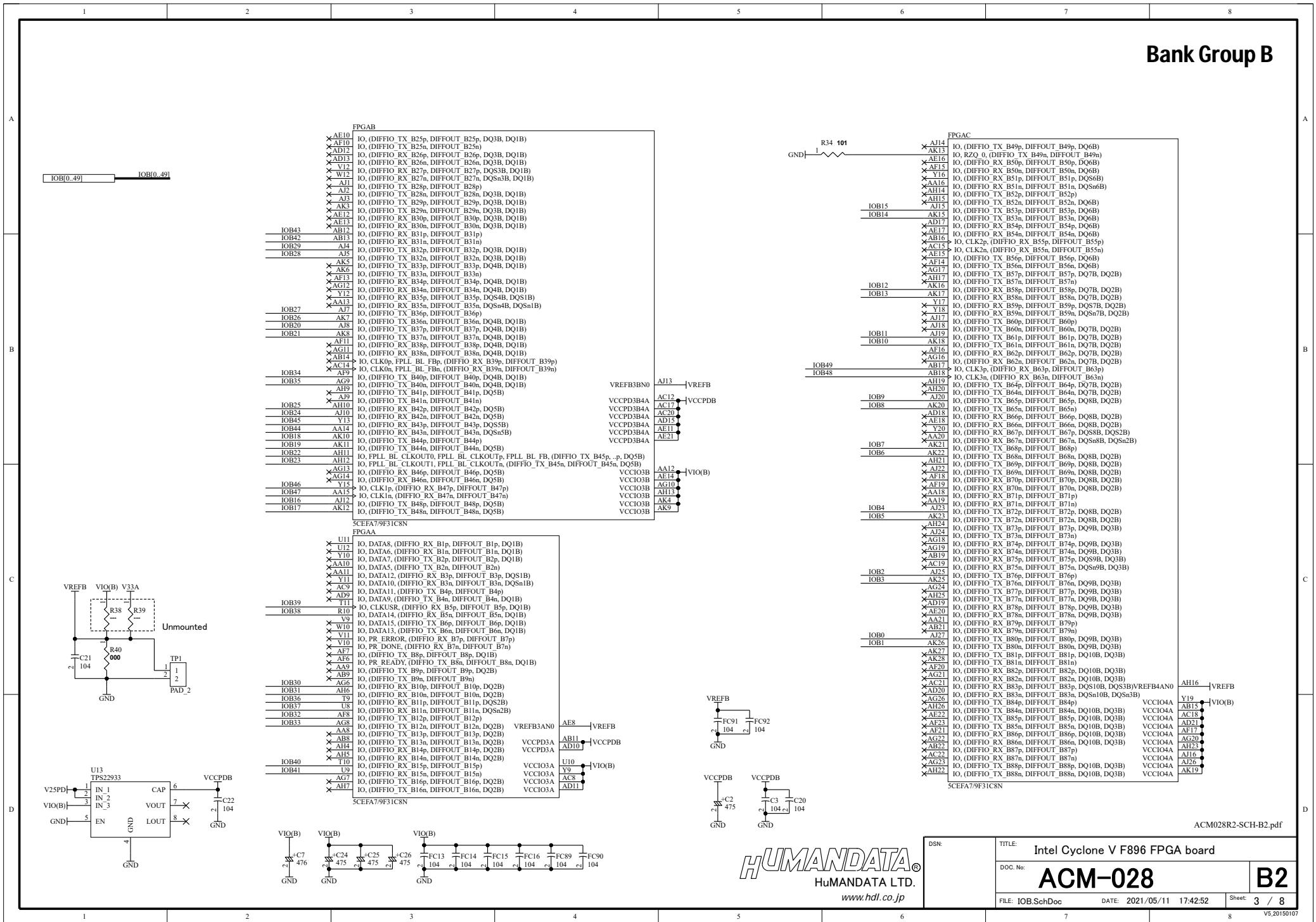
D

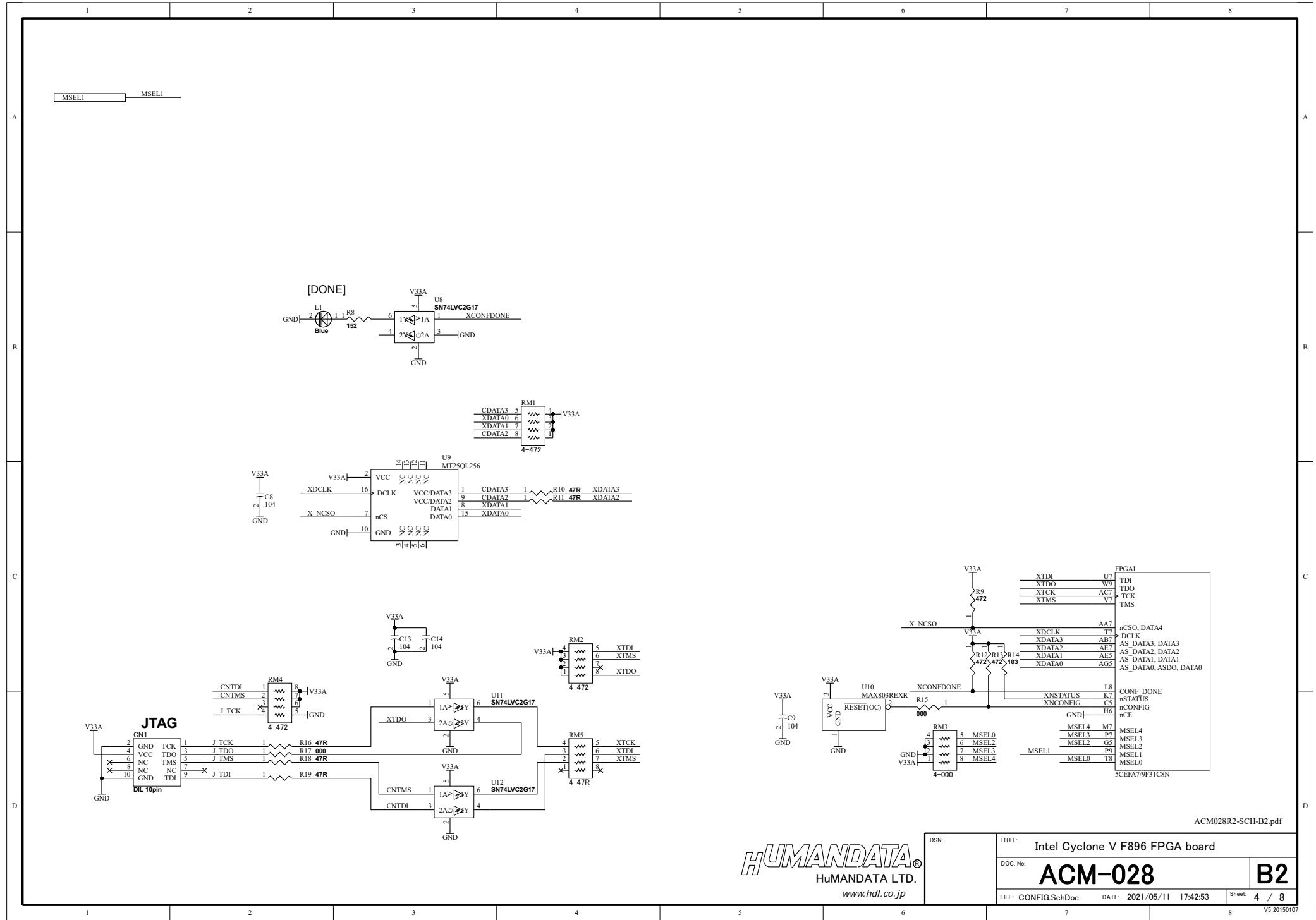


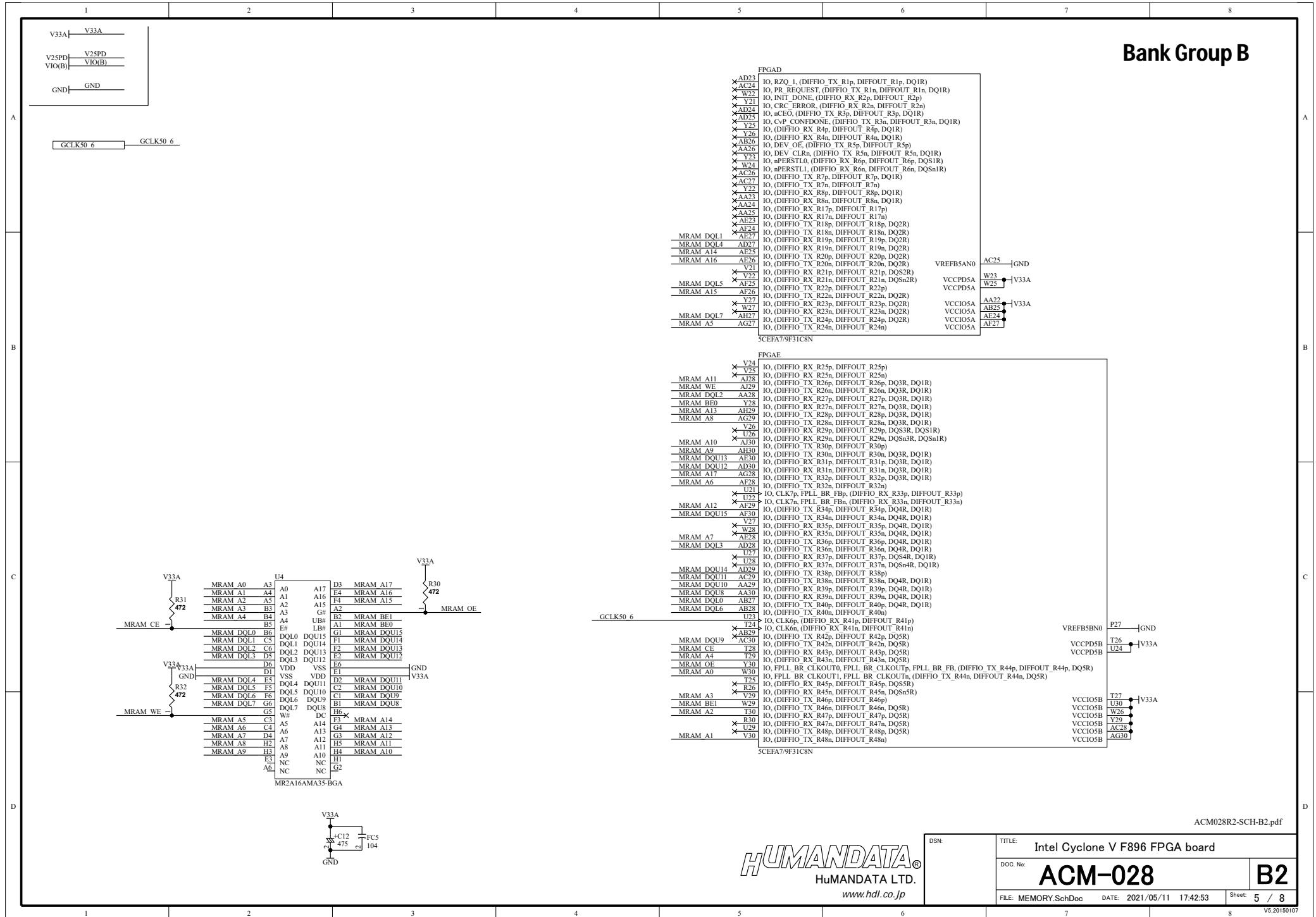
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Bank Group B

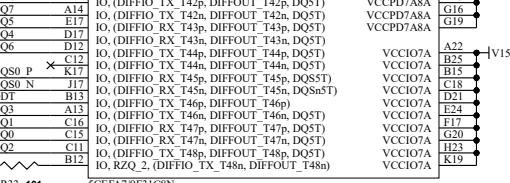
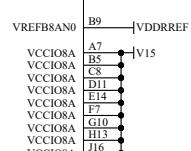
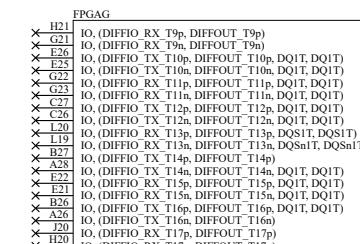
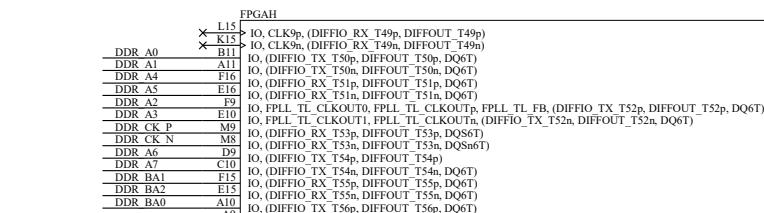






GCLK50_8 GCLK50_8

A

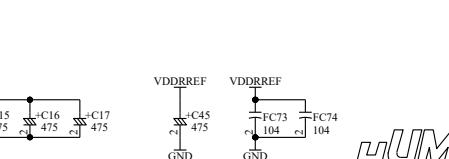


DDR A[0..14]	DDR A0[0..2]	DDR BA[0..31]	DDR BA[0..2]
DDR DQ0[0..31]	DDR DQ0[0..2]	DDR RAS	DDR RAS
DDR DQ1[0..31]	DDR DQ1[0..2]	DDR CAS	DDR CAS
DDR DQ2[0..31]	DDR DQ2[0..2]	DDR WE	DDR WE
DDR DQ3[0..31]	DDR DQ3[0..2]	DDR CK_P	DDR CK_N
DDR DQ4[0..31]	DDR DQ4[0..2]	DDR CKE	DDR OKE
DDR DQ5[0..31]	DDR DQ5[0..2]	DDR RESET	DDR RESET
DDR DQ6[0..31]	DDR DQ6[0..2]	DDR ODT	DDR ODT
DDR DQ7[0..31]	DDR DQ7[0..2]	DDR CS	DDR CS
DDR DQ8[0..31]	DDR DQ8[0..2]	DDR DM0..3	DDR DM0..3
DDR DQ9[0..31]	DDR DQ9[0..2]	DDR DQ50_P	DDR DQ50_N
DDR DQ10[0..31]	DDR DQ10[0..2]	DDR DQ50_N	DDR DQ50_P
DDR DQ11[0..31]	DDR DQ11[0..2]	DDR DQ51_P	DDR DQ51_N
DDR DQ12[0..31]	DDR DQ12[0..2]	DDR DQ51_N	DDR DQ52_P
DDR DQ13[0..31]	DDR DQ13[0..2]	DDR DQ52_P	DDR DQ52_N
DDR DQ14[0..31]	DDR DQ14[0..2]	DDR DQ52_N	DDR DQ53_P
DDR DQ15[0..31]	DDR DQ15[0..2]	DDR DQ53_P	DDR DQ53_N

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