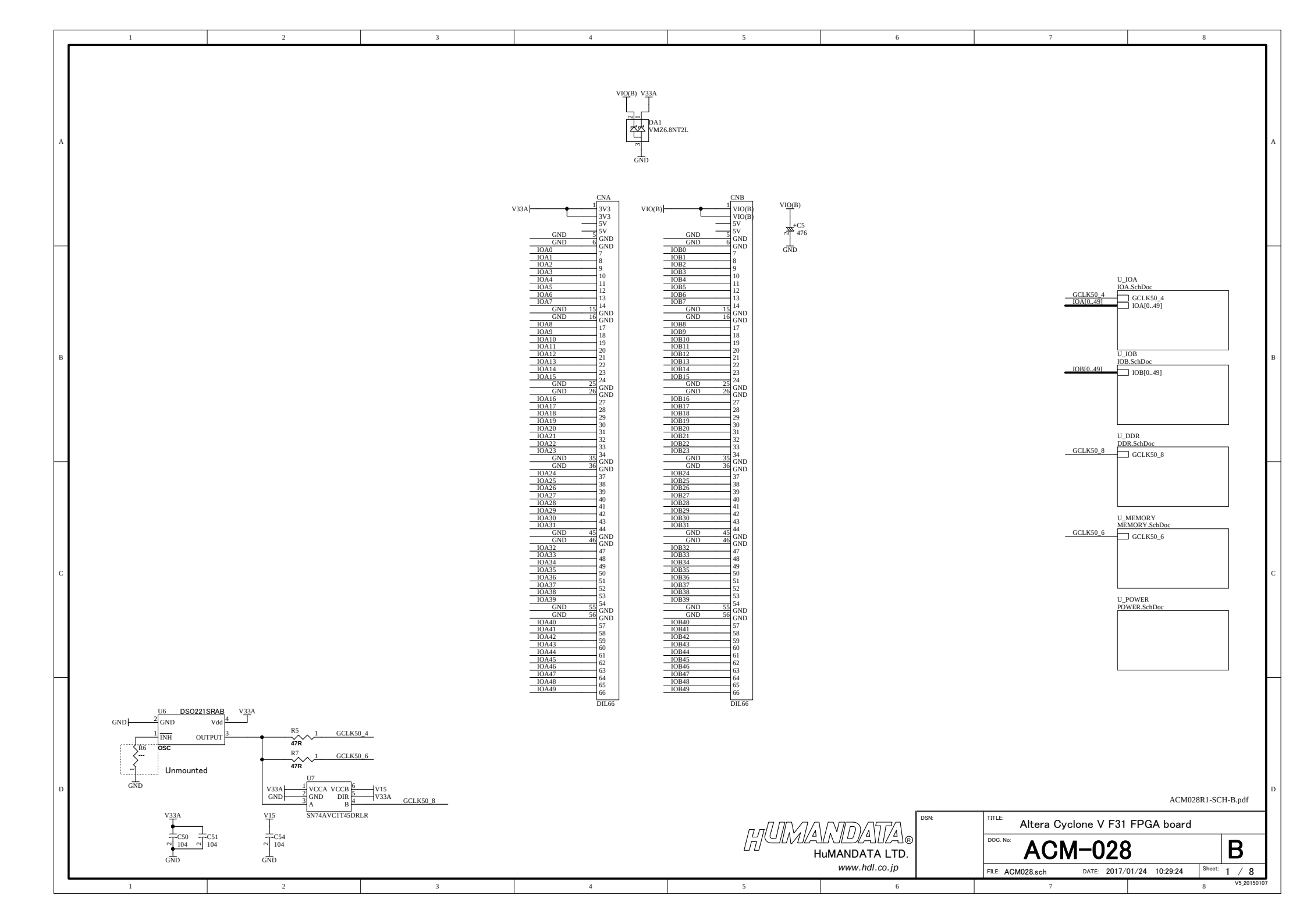

ACM028R1-SCH-B.pdf

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DSN:	TITLE: Altera Cyclone V F31 FPGA board	
	DOC. No: ACM-028	B
	FILE: ACM028.sch DATE: 2017/01/24 10:29:24	Sheet: 1 / 8

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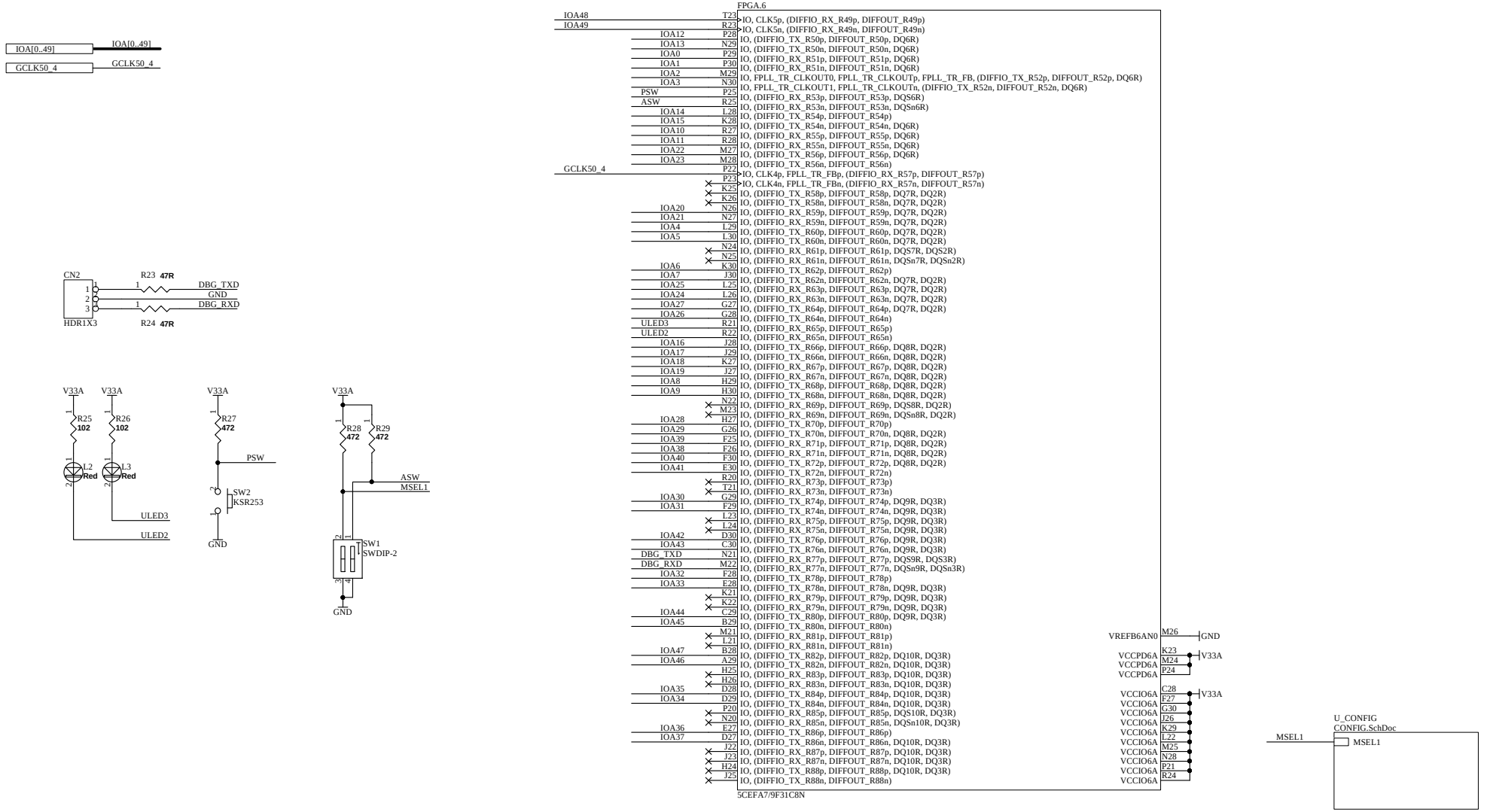
Bank Group A(3.3V)



ACM028R1-SCH-B.pdf

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DSN:	
TITLE:	Altera Cyclone V F31 FPGA board
DOC. No:	ACM-028 B
FILE:	IOA.SchDoc
DATE:	2017/01/24 10:29:24
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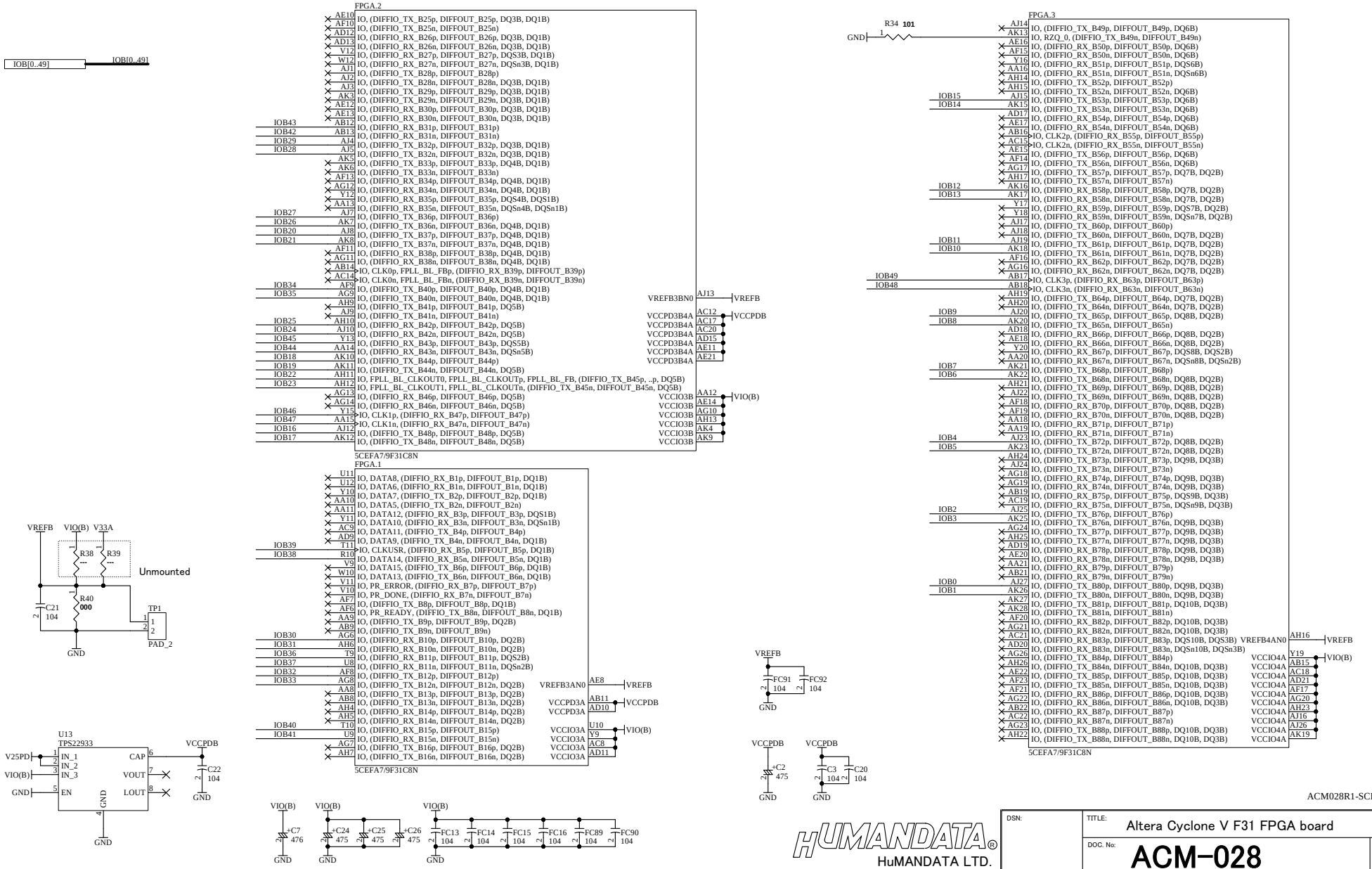
Bank Group B



ACM028R1-SCH-B.pdf

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DSN:	TITLE: Altera Cyclone V F31 FPGA board	
	DOC. No: ACM-028	B
	FILE: IOB.SchDoc DATE: 2017/01/24 10:29:24	Sheet: 3 / 8

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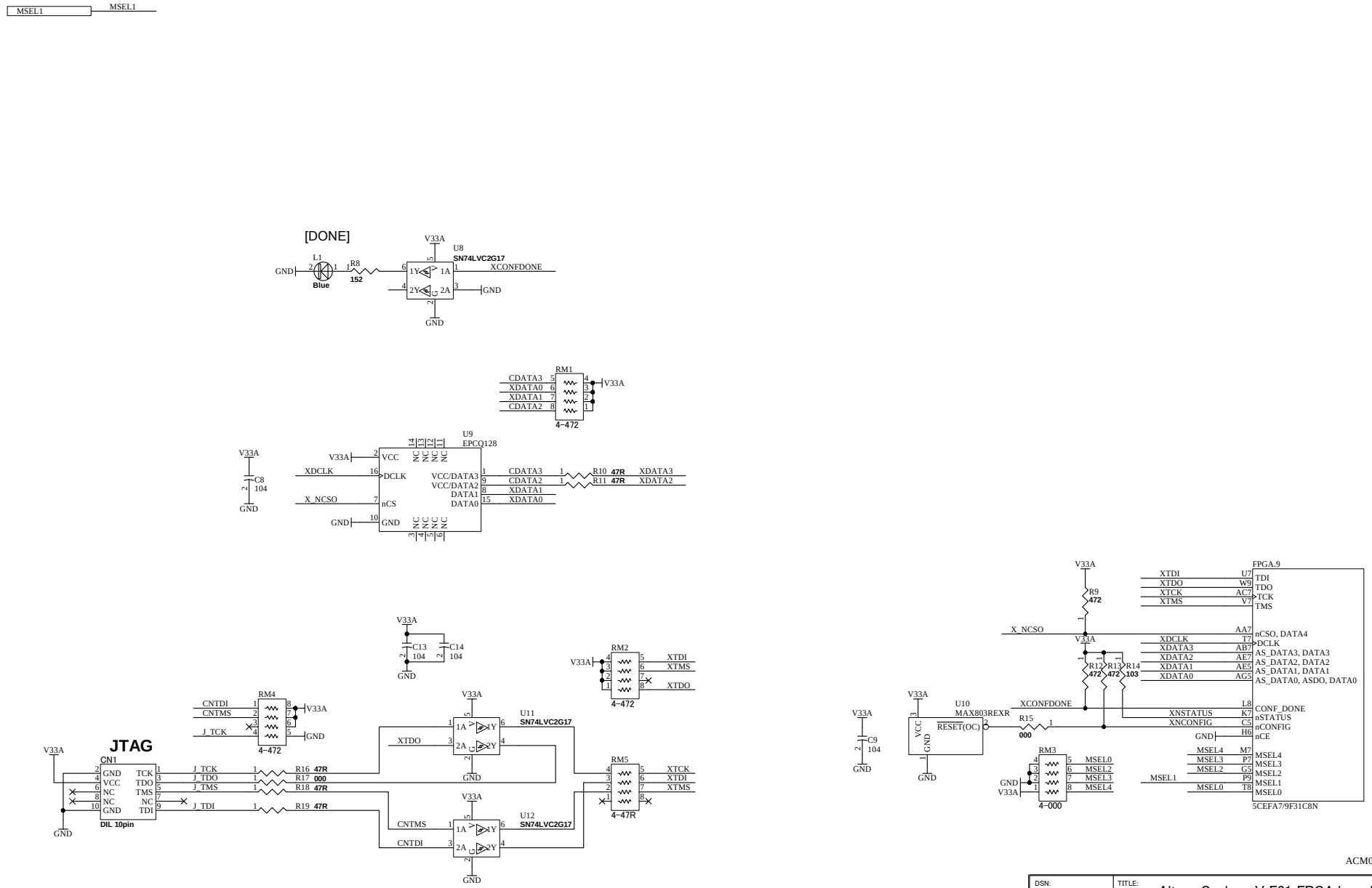
MSEL1
MSEL1
[DONE]
L1
Blue
R8
152
GND
V33A
U8
SN74LVC2G17
XCONFDONE
GND
RM1
CDATA3
XDATA0
XDATA1
CDATA2
4-472
V33A
U9
EPCQ128
VCC
DCLK
nCS
GND
XDCLK
X_NCSO
VCC/DATA3
VCC/DATA2
DATA1
DATA0
CDATA3
CDATA2
XDATA1
XDATA0
R10 47R
R11 47R
XDATA3
XDATA2
C8
104
C13
104
C14
104
RM2
4-472
XTDI
XTMS
XTDO
RM4
CNTDI
CNTMS
J_TCK
4-472
U11
SN74LVC2G17
U12
SN74LVC2G17
JTAG
CN1
GND
VCC
NC
NC
TCK
TDO
TMS
NC
TDI
DIL 10pin
J_TCK
J_TDO
J_TMS
J_TDI
R16 47R
R17 000
R18 47R
R19 47R
RM5
4-47R
XTCK
XTDI
XTMS
CNTMS
CNTDI
C9
104
U10
MAX803REXR
RESET(OC)
R15
000
XCONFDONE
R9
472
R12 472
R13 472
R14 103
RM3
4-000
MSEL0
MSEL2
MSEL3
MSEL4
MSEL1
MSEL4
MSEL3
MSEL2
MSEL1
MSEL0
FPGA.9
XTDI
XTDO
XTCK
XTMS
TDI
TDO
TCK
TMS
X_NCSO
nCSO, DATA4
DCLK
XDCLK
XDATA3
XDATA2
XDATA1
XDATA0
AS_DATA3, DATA3
AS_DATA2, DATA2
AS_DATA1, DATA1
AS_DATA0, ASDO, DATA0
CONF_DONE
nSTATUS
nCONFIG
nCE
XNSTATUS
XNCONFIG
5CEFA7/9F31C8N
ACM028R1-SCH-B.pdf
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DSN:
TITLE: Altera Cyclone V F31 FPGA board
DOC. No: ACM-028
B
FILE: CONFIG.SchDoc
DATE: 2017/01/24 10:29:24
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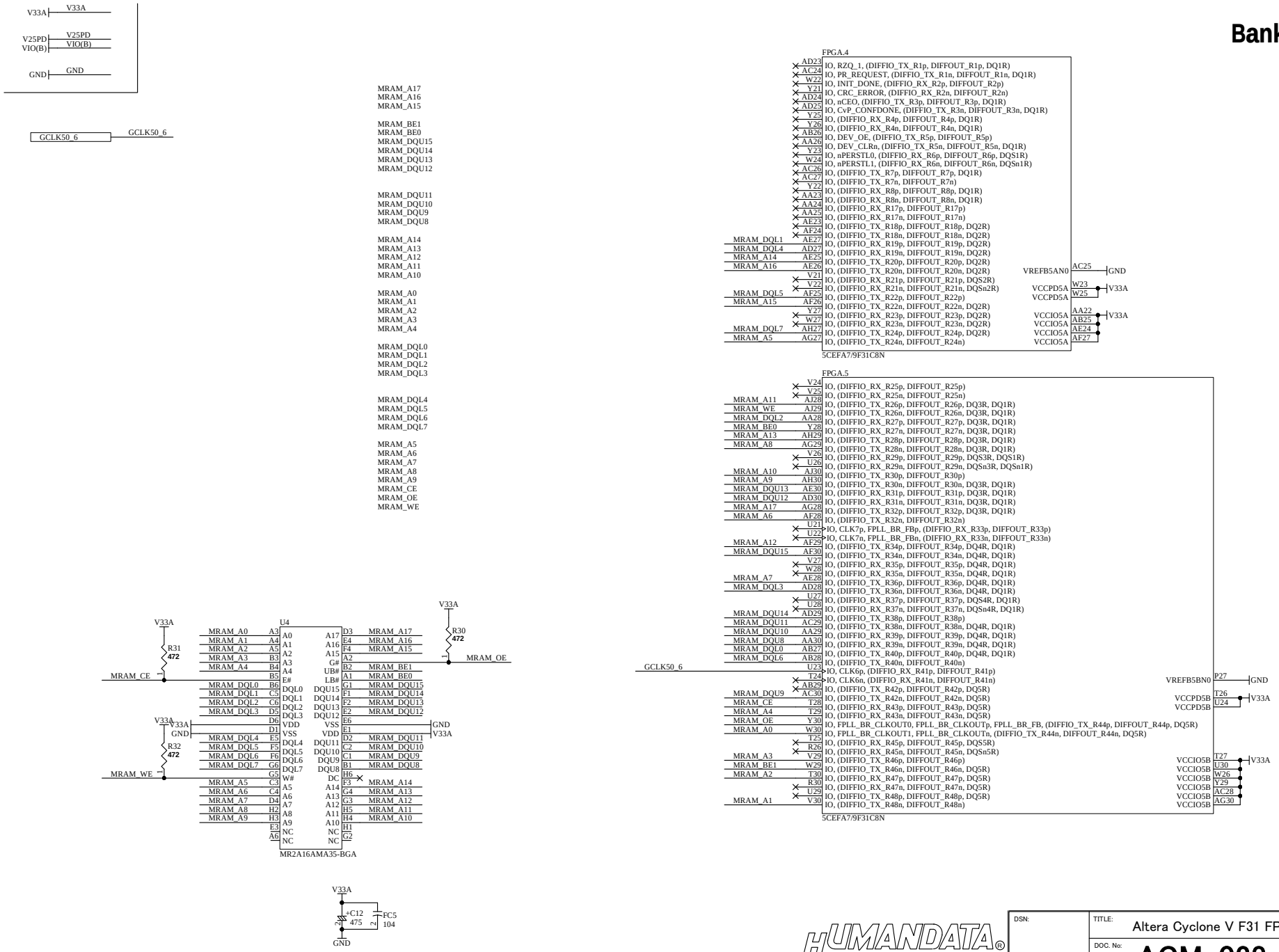
Bank Group B


V33A
V25PD
VIO(B)
GND
GCLK50_6
MRAM_A17
MRAM_A16
MRAM_A15
MRAM_BE1
MRAM_BE0
MRAM_DQU15
MRAM_DQU14
MRAM_DQU13
MRAM_DQU12
MRAM_DQU11
MRAM_DQU10
MRAM_DQU9
MRAM_DQU8
MRAM_A14
MRAM_A13
MRAM_A12
MRAM_A11
MRAM_A10
MRAM_A0
MRAM_A1
MRAM_A2
MRAM_A3
MRAM_A4
MRAM_DQL0
MRAM_DQL1
MRAM_DQL2
MRAM_DQL3
MRAM_DQL4
MRAM_DQL5
MRAM_DQL6
MRAM_DQL7
MRAM_A5
MRAM_A6
MRAM_A7
MRAM_A8
MRAM_A9
MRAM_CE
MRAM_OE
MRAM_WE
FPGA.4
IO, RZQ_1, (DIFFIO_TX_R1p, DIFFOUT_R1p, DQ1R)
IO, PR_REQUEST, (DIFFIO_TX_R1n, DIFFOUT_R1n, DQ1R)
IO, INIT_DONE, (DIFFIO_RX_R2p, DIFFOUT_R2p)
IO, CRC_ERROR, (DIFFIO_RX_R2n, DIFFOUT_R2n)
IO, nCEO, (DIFFIO_TX_R3p, DIFFOUT_R3p, DQ1R)
IO, CvP_CONFDONE, (DIFFIO_TX_R3n, DIFFOUT_R3n, DQ1R)
IO, (DIFFIO_RX_R4p, DIFFOUT_R4p, DQ1R)
IO, (DIFFIO_RX_R4n, DIFFOUT_R4n, DQ1R)
IO, DEV_OE, (DIFFIO_TX_R5p, DIFFOUT_R5p)
IO, DEV_CLRn, (DIFFIO_TX_R5n, DIFFOUT_R5n, DQ1R)
IO, nPERSTL0, (DIFFIO_RX_R6p, DIFFOUT_R6p, DQS1R)
IO, nPERSTL1, (DIFFIO_RX_R6n, DIFFOUT_R6n, DQSn1R)
IO, (DIFFIO_TX_R7p, DIFFOUT_R7p, DQ1R)
IO, (DIFFIO_TX_R7n, DIFFOUT_R7n)
IO, (DIFFIO_RX_R8p, DIFFOUT_R8p, DQ1R)
IO, (DIFFIO_RX_R8n, DIFFOUT_R8n, DQ1R)
IO, (DIFFIO_RX_R17p, DIFFOUT_R17p)
IO, (DIFFIO_RX_R17n, DIFFOUT_R17n)
IO, (DIFFIO_TX_R18p, DIFFOUT_R18p, DQ2R)
IO, (DIFFIO_TX_R18n, DIFFOUT_R18n, DQ2R)
IO, (DIFFIO_RX_R19p, DIFFOUT_R19p, DQ2R)
IO, (DIFFIO_RX_R19n, DIFFOUT_R19n, DQ2R)
IO, (DIFFIO_TX_R20p, DIFFOUT_R20p, DQ2R)
IO, (DIFFIO_TX_R20n, DIFFOUT_R20n, DQ2R)
IO, (DIFFIO_RX_R21p, DIFFOUT_R21p, DQS2R)
IO, (DIFFIO_RX_R21n, DIFFOUT_R21n, DQSn2R)
IO, (DIFFIO_TX_R22p, DIFFOUT_R22p)
IO, (DIFFIO_TX_R22n, DIFFOUT_R22n, DQ2R)
IO, (DIFFIO_RX_R23p, DIFFOUT_R23p, DQ2R)
IO, (DIFFIO_RX_R23n, DIFFOUT_R23n, DQ2R)
IO, (DIFFIO_TX_R24p, DIFFOUT_R24p, DQ2R)
IO, (DIFFIO_TX_R24n, DIFFOUT_R24n)
VREFB5AN0
VCCPD5A
VCCIO5A
5CEFA7/9F31C8N
FPGA.5
IO, (DIFFIO_RX_R25p, DIFFOUT_R25p)
IO, (DIFFIO_RX_R25n, DIFFOUT_R25n)
IO, (DIFFIO_TX_R26p, DIFFOUT_R26p, DQ3R, DQ1R)
IO, (DIFFIO_TX_R26n, DIFFOUT_R26n, DQ3R, DQ1R)
IO, (DIFFIO_TX_R27p, DIFFOUT_R27p, DQ3R, DQ1R)
IO, (DIFFIO_TX_R27n, DIFFOUT_R27n, DQ3R, DQ1R)
IO, (DIFFIO_TX_R28p, DIFFOUT_R28p, DQ3R, DQ1R)
IO, (DIFFIO_TX_R28n, DIFFOUT_R28n, DQ3R, DQ1R)
IO, (DIFFIO_RX_R29p, DIFFOUT_R29p, DQS3R, DQS1R)
IO, (DIFFIO_RX_R29n, DIFFOUT_R29n, DQSn3R, DQSn1R)
IO, (DIFFIO_TX_R30p, DIFFOUT_R30p)
IO, (DIFFIO_TX_R30n, DIFFOUT_R30n, DQ3R, DQ1R)
IO, (DIFFIO_TX_R31p, DIFFOUT_R31p, DQ3R, DQ1R)
IO, (DIFFIO_TX_R31n, DIFFOUT_R31n, DQ3R, DQ1R)
IO, (DIFFIO_TX_R32p, DIFFOUT_R32p, DQ3R, DQ1R)
IO, (DIFFIO_TX_R32n, DIFFOUT_R32n)
IO, CLK7p, FPLL_BR_FBp, (DIFFIO_RX_R33p, DIFFOUT_R33p)
IO, CLK7n, FPLL_BR_FBn, (DIFFIO_RX_R33n, DIFFOUT_R33n)
IO, (DIFFIO_TX_R34p, DIFFOUT_R34p, DQ4R, DQ1R)
IO, (DIFFIO_TX_R34n, DIFFOUT_R34n, DQ4R, DQ1R)
IO, (DIFFIO_RX_R35p, DIFFOUT_R35p, DQ4R, DQ1R)
IO, (DIFFIO_RX_R35n, DIFFOUT_R35n, DQ4R, DQ1R)
IO, (DIFFIO_TX_R36p, DIFFOUT_R36p, DQ4R, DQ1R)
IO, (DIFFIO_TX_R36n, DIFFOUT_R36n, DQ4R, DQ1R)
IO, (DIFFIO_TX_R37p, DIFFOUT_R37p, DQS4R, DQ1R)
IO, (DIFFIO_RX_R37n, DIFFOUT_R37n, DQSn4R, DQ1R)
IO, (DIFFIO_TX_R38p, DIFFOUT_R38p)
IO, (DIFFIO_TX_R38n, DIFFOUT_R38n, DQ4R, DQ1R)
IO, (DIFFIO_RX_R39p, DIFFOUT_R39p, DQ4R, DQ1R)
IO, (DIFFIO_RX_R39n, DIFFOUT_R39n, DQ4R, DQ1R)
IO, (DIFFIO_TX_R40p, DIFFOUT_R40p, DQ4R, DQ1R)
IO, (DIFFIO_TX_R40n, DIFFOUT_R40n)
IO, CLK6p, (DIFFIO_RX_R41p, DIFFOUT_R41p)
IO, CLK6n, (DIFFIO_RX_R41n, DIFFOUT_R41n)
IO, (DIFFIO_TX_R42p, DIFFOUT_R42p, DQ5R)
IO, (DIFFIO_TX_R42n, DIFFOUT_R42n, DQ5R)
IO, (DIFFIO_RX_R43p, DIFFOUT_R43p, DQ5R)
IO, (DIFFIO_RX_R43n, DIFFOUT_R43n, DQ5R)
IO, FPLL_BR_CLKOUT0, FPLL_BR_CLKOUTp, FPLL_BR_FB, (DIFFIO_TX_R44p, DIFFOUT_R44p, DQ5R)
IO, FPLL_BR_CLKOUT1, FPLL_BR_CLKOUTn, (DIFFIO_TX_R44n, DIFFOUT_R44n, DQ5R)
IO, (DIFFIO_RX_R45p, DIFFOUT_R45p, DQS5R)
IO, (DIFFIO_RX_R45n, DIFFOUT_R45n, DQSn5R)
IO, (DIFFIO_TX_R46p, DIFFOUT_R46p)
IO, (DIFFIO_TX_R46n, DIFFOUT_R46n, DQ5R)
IO, (DIFFIO_TX_R47p, DIFFOUT_R47p, DQ5R)
IO, (DIFFIO_TX_R47n, DIFFOUT_R47n, DQ5R)
IO, (DIFFIO_TX_R48p, DIFFOUT_R48p, DQ5R)
IO, (DIFFIO_TX_R48n, DIFFOUT_R48n)
VREFB5BN0
VCCPD5B
VCCIO5B
5CEFA7/9F31C8N
U4
MR2A16AMA35-BGA
R31
R32
R30
472
C12
475
C5
104
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TITLE: Altera Cyclone V F31 FPGA board
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GCLK50_8 — GCLK50_8

FPGA.8

	L15	IO, CLK9p, (DIFFIO_RX_T49p, DIFFOUT_T49p)
	K15	IO, CLK9n, (DIFFIO_RX_T49n, DIFFOUT_T49n)
DDR_A0	B11	IO, (DIFFIO_TX_T50p, DIFFOUT_T50p, DQ6T)
DDR_A1	A11	IO, (DIFFIO_TX_T50n, DIFFOUT_T50n, DQ6T)
DDR_A4	F16	IO, (DIFFIO_RX_T51p, DIFFOUT_T51p, DQ6T)
DDR_A5	E16	IO, (DIFFIO_RX_T51n, DIFFOUT_T51n, DQ6T)
DDR_A2	F9	IO, FPLL_TL_CLKOUT0, FPLL_TL_CLKOUTp, FPLL_TL_FB, (DIFFIO_TX_T52p, DIFFOUT_T52p, DQ6T)
DDR_A3	E10	IO, FPLL_TL_CLKOUT1, FPLL_TL_CLKOUTn, (DIFFIO_TX_T52n, DIFFOUT_T52n, DQ6T)
DDR_CK_P	M9	IO, (DIFFIO_RX_T53p, DIFFOUT_T53p, DQS6T)
DDR_CK_N	M8	IO, (DIFFIO_RX_T53n, DIFFOUT_T53n, DQSn6T)
DDR_A6	D9	IO, (DIFFIO_TX_T54p, DIFFOUT_T54p)
DDR_A7	C10	IO, (DIFFIO_TX_T54n, DIFFOUT_T54n, DQ6T)
DDR_BA1	F15	IO, (DIFFIO_RX_T55p, DIFFOUT_T55p, DQ6T)
DDR_BA2	E15	IO, (DIFFIO_RX_T55n, DIFFOUT_T55n, DQ6T)
DDR_BA0	A10	IO, (DIFFIO_TX_T56p, DIFFOUT_T56p, DQ6T)
	A9	IO, (DIFFIO_TX_T56n, DIFFOUT_T56n)
GCLK50_8	L14	IO, CLK8p, FPLL_TL_FBp, (DIFFIO_RX_T57p, DIFFOUT_T57p)
	L13	IO, CLK8n, FPLL_TL_FBn, (DIFFIO_RX_T57n, DIFFOUT_T57n)
DDR_CAS	C9	IO, (DIFFIO_TX_T58p, DIFFOUT_T58p, DQ7T)
DDR_RAS	B8	IO, (DIFFIO_TX_T58n, DIFFOUT_T58n, DQ7T)
DDR_A8	E12	IO, (DIFFIO_RX_T59p, DIFFOUT_T59p, DQ7T)
DDR_A9	D13	IO, (DIFFIO_RX_T59n, DIFFOUT_T59n, DQ7T)
DDR_A10	B7	IO, (DIFFIO_TX_T60p, DIFFOUT_T60p, DQ7T)
DDR_A11	A8	IO, (DIFFIO_TX_T60n, DIFFOUT_T60n, DQ7T)
DDR_CS	J15	IO, (DIFFIO_RX_T61p, DIFFOUT_T61p, DQS7T)
	H15	IO, (DIFFIO_RX_T61n, DIFFOUT_T61n, DQSn7T)
DDR_A12	B6	IO, (DIFFIO_TX_T62p, DIFFOUT_T62p)
DDR_A13	A6	IO, (DIFFIO_TX_T62n, DIFFOUT_T62n, DQ7T)
DDR_A14	E11	IO, (DIFFIO_RX_T63p, DIFFOUT_T63p, DQ7T)
	D10	IO, (DIFFIO_RX_T63n, DIFFOUT_T63n, DQ7T)
DDR_WE	C7	IO, (DIFFIO_TX_T64p, DIFFOUT_T64p, DQ7T)
	C6	IO, (DIFFIO_TX_T64n, DIFFOUT_T64n)
	L10	IO, (DIFFIO_RX_T65p, DIFFOUT_T65p)
	L9	IO, (DIFFIO_RX_T65n, DIFFOUT_T65n)
	F13	IO, (DIFFIO_TX_T66p, DIFFOUT_T66p, DQ8T)
	E13	IO, (DIFFIO_TX_T66n, DIFFOUT_T66n, DQ8T)
	G14	IO, (DIFFIO_RX_T67p, DIFFOUT_T67p, DQ8T)
	F14	IO, (DIFFIO_RX_T67n, DIFFOUT_T67n, DQ8T)
	A5	IO, (DIFFIO_TX_T68p, DIFFOUT_T68p, DQ8T)
	A4	IO, (DIFFIO_TX_T68n, DIFFOUT_T68n, DQ8T)
	J14	IO, (DIFFIO_RX_T69p, DIFFOUT_T69p, DQS8T)
	H14	IO, (DIFFIO_RX_T69n, DIFFOUT_T69n, DQSn8T)
	J7	IO, (DIFFIO_TX_T70p, DIFFOUT_T70p)
	H7	IO, (DIFFIO_TX_T70n, DIFFOUT_T70n, DQ8T)
	L11	IO, (DIFFIO_RX_T71p, DIFFOUT_T71p, DQ8T)
	K11	IO, (DIFFIO_RX_T71n, DIFFOUT_T71n, DQ8T)
	J9	IO, (DIFFIO_TX_T72p, DIFFOUT_T72p, DQ8T)
	H9	IO, (DIFFIO_TX_T72n, DIFFOUT_T72n)
	P12	IO, (DIFFIO_RX_T73p, DIFFOUT_T73p)
	N12	IO, (DIFFIO_RX_T73n, DIFFOUT_T73n)
	G9	IO, (DIFFIO_TX_T74p, DIFFOUT_T74p, DQ9T, DQ3T)
	F8	IO, (DIFFIO_TX_T74n, DIFFOUT_T74n, DQ9T, DQ3T)
	H12	IO, (DIFFIO_RX_T75p, DIFFOUT_T75p, DQ9T, DQ3T)
	G12	IO, (DIFFIO_RX_T75n, DIFFOUT_T75n, DQ9T, DQ3T)
	E8	IO, (DIFFIO_TX_T76p, DIFFOUT_T76p, DQ9T, DQ3T)
	D8	IO, (DIFFIO_TX_T76n, DIFFOUT_T76n, DQ9T, DQ3T)
	K13	IO, (DIFFIO_RX_T77p, DIFFOUT_T77p, DQS9T, DQS3T)
	J13	IO, (DIFFIO_RX_T77n, DIFFOUT_T77n, DQSn9T, DQSn3T)
	A3	IO, (DIFFIO_TX_T78p, DIFFOUT_T78p)
	A2	IO, (DIFFIO_TX_T78n, DIFFOUT_T78n, DQ9T, DQ3T)
	P10	IO, (DIFFIO_RX_T79p, DIFFOUT_T79p, DQ9T, DQ3T)
	N11	IO, (DIFFIO_RX_T79n, DIFFOUT_T79n, DQ9T, DQ3T)
	D7	IO, (DIFFIO_TX_T80p, DIFFOUT_T80p, DQ9T, DQ3T)
	D6	IO, (DIFFIO_TX_T80n, DIFFOUT_T80n)
	R12	IO, (DIFFIO_RX_T81p, DIFFOUT_T81p)
	R11	IO, (DIFFIO_RX_T81n, DIFFOUT_T81n)
	E7	IO, (DIFFIO_TX_T82p, DIFFOUT_T82p, DQ10T, DQ3T)
	E6	IO, (DIFFIO_TX_T82n, DIFFOUT_T82n, DQ10T, DQ3T)
	K12	IO, (DIFFIO_RX_T83p, DIFFOUT_T83p, DQ10T, DQ3T)
	J12	IO, (DIFFIO_RX_T83n, DIFFOUT_T83n, DQ10T, DQ3T)
	K10	IO, (DIFFIO_TX_T84p, DIFFOUT_T84p, DQ10T, DQ3T)
	J10	IO, (DIFFIO_TX_T84n, DIFFOUT_T84n, DQ10T, DQ3T)
	N10	IO, (DIFFIO_RX_T85p, DIFFOUT_T85p, DQS10T, DQ3T)
	N9	IO, (DIFFIO_RX_T85n, DIFFOUT_T85n, DQSn10T, DQ3T)
	G6	IO, (DIFFIO_TX_T86p, DIFFOUT_T86p)
	F6	IO, (DIFFIO_TX_T86n, DIFFOUT_T86n, DQ10T, DQ3T)
	M12	IO, (DIFFIO_RX_T87p, DIFFOUT_T87p, DQ10T, DQ3T)
	M11	IO, (DIFFIO_RX_T87n, DIFFOUT_T87n, DQ10T, DQ3T)
	G8	IO, (DIFFIO_TX_T88p, DIFFOUT_T88p, DQ10T, DQ3T)
	G7	IO, (DIFFIO_TX_T88n, DIFFOUT_T88n)

5CEFA7/9F31C8N

VREFB8AN0	B9	VDDRREF
VCCIO8A	A7	V15
VCCIO8A	B5	
VCCIO8A	C8	
VCCIO8A	D11	
VCCIO8A	E14	
VCCIO8A	F7	
VCCIO8A	G10	
VCCIO8A	H13	
VCCIO8A	J16	
VCCIO8A	L12	

FPGA.7

	H21	IO, (DIFFIO_RX_T9p, DIFFOUT_T9p)
	G21	IO, (DIFFIO_RX_T9n, DIFFOUT_T9n)
	E26	IO, (DIFFIO_TX_T10p, DIFFOUT_T10p, DQ1T, DQ1T)
	E25	IO, (DIFFIO_TX_T10n, DIFFOUT_T10n, DQ1T, DQ1T)
	G22	IO, (DIFFIO_RX_T11p, DIFFOUT_T11p, DQ1T, DQ1T)
	G23	IO, (DIFFIO_RX_T11n, DIFFOUT_T11n, DQ1T, DQ1T)
	C27	IO, (DIFFIO_TX_T12p, DIFFOUT_T12p, DQ1T, DQ1T)
	C26	IO, (DIFFIO_TX_T12n, DIFFOUT_T12n, DQ1T, DQ1T)
	L20	IO, (DIFFIO_RX_T13p, DIFFOUT_T13p, DQS1T, DQS1T)
	L19	IO, (DIFFIO_RX_T13n, DIFFOUT_T13n, DQSn1T, DQSn1T)
	B27	IO, (DIFFIO_TX_T14p, DIFFOUT_T14p)
	A28	IO, (DIFFIO_TX_T14n, DIFFOUT_T14n, DQ1T, DQ1T)
	E22	IO, (DIFFIO_RX_T15p, DIFFOUT_T15p, DQ1T, DQ1T)
	E21	IO, (DIFFIO_RX_T15n, DIFFOUT_T15n, DQ1T, DQ1T)
	B26	IO, (DIFFIO_TX_T16p, DIFFOUT_T16p, DQ1T, DQ1T)
	A26	IO, (DIFFIO_TX_T16n, DIFFOUT_T16n)
	J20	IO, (DIFFIO_RX_T17p, DIFFOUT_T17p)
	H20	IO, (DIFFIO_RX_T17n, DIFFOUT_T17n)
DDR_DM3	D25	IO, (DIFFIO_TX_T18p, DIFFOUT_T18p, DQ2T, DQ1T)
DDR_DQ31	C25	IO, (DIFFIO_TX_T18n, DIFFOUT_T18n, DQ2T, DQ1T)
DDR_DQ29	C21	IO, (DIFFIO_RX_T19p, DIFFOUT_T19p, DQ2T, DQ1T)
DDR_DQ28	C20	IO, (DIFFIO_RX_T19n, DIFFOUT_T19n, DQ2T, DQ1T)
DDR_DQ30	D23	IO, (DIFFIO_TX_T20p, DIFFOUT_T20p, DQ2T, DQ1T)
	C22	IO, (DIFFIO_TX_T20n, DIFFOUT_T20n, DQ2T, DQ1T)
DDR_DQS3_P	K20	IO, (DIFFIO_RX_T21p, DIFFOUT_T21p, DQS2T, DQ1T)
DDR_DQS3_N	J19	IO, (DIFFIO_RX_T21n, DIFFOUT_T21n, DQSn2T, DQ1T)
	E23	IO, (DIFFIO_TX_T22p, DIFFOUT_T22p)
DDR_DQ27	D22	IO, (DIFFIO_TX_T22n, DIFFOUT_T22n, DQ2T, DQ1T)
DDR_DQ25	D20	IO, (DIFFIO_RX_T23p, DIFFOUT_T23p, DQ2T, DQ1T)
DDR_DQ24	C19	IO, (DIFFIO_RX_T23n, DIFFOUT_T23n, DQ2T, DQ1T)
DDR_DQ26	A25	IO, (DIFFIO_TX_T24p, DIFFOUT_T24p, DQ2T, DQ1T)
	A24	IO, (DIFFIO_TX_T24n, DIFFOUT_T24n)
	F20	IO, (DIFFIO_RX_T25p, DIFFOUT_T25p)
	E20	IO, (DIFFIO_RX_T25n, DIFFOUT_T25n)
DDR_DM2	C24	IO, (DIFFIO_TX_T26p, DIFFOUT_T26p, DQ3T, DQ2T)
DDR_DQ23	B24	IO, (DIFFIO_TX_T26n, DIFFOUT_T26n, DQ3T, DQ2T)
DDR_DQ21	F19	IO, (DIFFIO_RX_T27p, DIFFOUT_T27p, DQ3T, DQ2T)
DDR_DQ20	E18	IO, (DIFFIO_RX_T27n, DIFFOUT_T27n, DQ3T, DQ2T)
DDR_DQ22	B23	IO, (DIFFIO_TX_T28p, DIFFOUT_T28p, DQ3T, DQ2T)
	A23	IO, (DIFFIO_TX_T28n, DIFFOUT_T28n, DQ3T, DQ2T)
DDR_DQS2_P	L18	IO, (DIFFIO_RX_T29p, DIFFOUT_T29p, DQS3T, DQS2T)
DDR_DQS2_N	K18	IO, (DIFFIO_RX_T29n, DIFFOUT_T29n, DQSn3T, DQSn2T)
DDR_RESET	B22	IO, (DIFFIO_TX_T30p, DIFFOUT_T30p)
DDR_DQ19	B21	IO, (DIFFIO_TX_T30n, DIFFOUT_T30n, DQ3T, DQ2T)
DDR_DQ17	D19	IO, (DIFFIO_RX_T31p, DIFFOUT_T31p, DQ3T, DQ2T)
DDR_DQ16	D18	IO, (DIFFIO_RX_T31n, DIFFOUT_T31n, DQ3T, DQ2T)
DDR_DQ18	A21	IO, (DIFFIO_TX_T32p, DIFFOUT_T32p, DQ3T, DQ2T)
	A20	IO, (DIFFIO_TX_T32n, DIFFOUT_T32n)
	H19	IO, CLK11p, (DIFFIO_RX_T33p, DIFFOUT_T33p)
	J18	IO, CLK11n, (DIFFIO_RX_T33n, DIFFOUT_T33n)
DDR_DM1	B19	IO, (DIFFIO_TX_T34p, DIFFOUT_T34p, DQ4T, DQ2T)
DDR_DQ15	A19	IO, (DIFFIO_TX_T34n, DIFFOUT_T34n, DQ4T, DQ2T)
DDR_DQ13	G18	IO, (DIFFIO_RX_T35p, DIFFOUT_T35p, DQ4T, DQ2T)
DDR_DQ12	F18	IO, (DIFFIO_RX_T35n, DIFFOUT_T35n, DQ4T, DQ2T)
DDR_DQ14	B18	IO, (DIFFIO_TX_T36p, DIFFOUT_T36p, DQ4T, DQ2T)
DDR_CKE	A18	IO, (DIFFIO_TX_T36n, DIFFOUT_T36n, DQ4T, DQ2T)
DDR_DQS1_P	K16	IO, (DIFFIO_RX_T37p, DIFFOUT_T37p, DQS4T, DQ2T)
DDR_DQS1_N	L16	IO, (DIFFIO_RX_T37n, DIFFOUT_T37n, DQSn4T, DQ2T)
	D14	IO, (DIFFIO_TX_T38p, DIFFOUT_T38p)
DDR_DQ11	C14	IO, (DIFFIO_TX_T38n, DIFFOUT_T38n, DQ4T, DQ2T)
DDR_DQ9	C17	IO, (DIFFIO_RX_T39p, DIFFOUT_T39p, DQ4T, DQ2T)
DDR_DQ8	B17	IO, (DIFFIO_RX_T39n, DIFFOUT_T39n, DQ4T, DQ2T)
DDR_DQ10	A16	IO, (DIFFIO_TX_T40p, DIFFOUT_T40p, DQ4T, DQ2T)
	A15	IO, (DIFFIO_TX_T40n, DIFFOUT_T40n)
	H17	IO, CLK10p, (DIFFIO_RX_T41p, DIFFOUT_T41p)
	G17	IO, CLK10n, (DIFFIO_RX_T41n, DIFFOUT_T41n)
DDR_DM0	B14	IO, (DIFFIO_TX_T42p, DIFFOUT_T42p, DQ5T)
DDR_DQ7	A14	IO, (DIFFIO_TX_T42n, DIFFOUT_T42n, DQ5T)
DDR_DQ5	E17	IO, (DIFFIO_RX_T43p, DIFFOUT_T43p, DQ5T)
DDR_DQ4	D17	IO, (DIFFIO_RX_T43n, DIFFOUT_T43n, DQ5T)
DDR_DQ6	D12	IO, (DIFFIO_TX_T44p, DIFFOUT_T44p, DQ5T)
	C12	IO, (DIFFIO_TX_T44n, DIFFOUT_T44n, DQ5T)
DDR_DQS0_P	K17	IO, (DIFFIO_RX_T45p, DIFFOUT_T45p, DQS5T)
DDR_DQS0_N	J17	IO, (DIFFIO_RX_T45n, DIFFOUT_T45n, DQSn5T)
DDR_ODT	B13	IO, (DIFFIO_TX_T46p, DIFFOUT_T46p)
DDR_DQ3	A13	IO, (DIFFIO_TX_T46n, DIFFOUT_T46n, DQ5T)
DDR_DQ1	C16	IO, (DIFFIO_RX_T47p, DIFFOUT_T47p, DQ5T)
DDR_DQ0	C15	IO, (DIFFIO_RX_T47n, DIFFOUT_T47n, DQ5T)
DDR_DQ2	C11	IO, (DIFFIO_TX_T48p, DIFFOUT_T48p, DQ5T)
GND	B12	IO, RZQ_2, (DIFFIO_TX_T48n, DIFFOUT_T48n)

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VREFB7AN0	B16	VDDRREF
VCCPD7A8A	D24	V25PD
VCCPD7A8A	F11	
VCCPD7A8A	F21	
VCCPD7A8A	F23	
VCCPD7A8A	G13	
VCCPD7A8A	G16	
VCCPD7A8A	G19	
VCCIO7A	A22	V15
VCCIO7A	B25	
VCCIO7A	B15	
VCCIO7A	C18	
VCCIO7A	D21	
VCCIO7A	E24	
VCCIO7A	F17	
VCCIO7A	G20	
VCCIO7A	H23	
VCCIO7A	K19	

U_DDR_MEM
DDR_MEM.SchDoc

DDR_A[0..14]	DDR_A[0..14]
DDR_DQ[0..31]	DDR_DQ[0..31]
DDR_BA[0..2]	DDR_BA[0..2]
DDR_RAS	DDR_RAS
DDR_CAS	DDR_CAS
DDR_WE	DDR_WE
DDR_CK_P	DDR_CK_P
DDR_CK_N	DDR_CK_N
DDR_CKE	DDR_CKE
DDR_RESET	DDR_RESET
DDR_ODT	DDR_ODT
DDR_CS	DDR_CS
DDR_DM[0..3]	DDR_DM[0..3]
DDR_DQS0_P	DDR_DQS0_P
DDR_DQS0_N	DDR_DQS0_N
DDR_DQS1_P	DDR_DQS1_P
DDR_DQS1_N	DDR_DQS1_N
DDR_DQS2_P	DDR_DQS2_P
DDR_DQS2_N	DDR_DQS2_N
DDR_DQS3_P	DDR_DQS3_P
DDR_DQS3_N	DDR_DQS3_N

V25PD: +C18 475, +C19 475 — GND
V25PD: FC53 104, FC54 104, FC55 104 — GND
V15: FC9 104, FC10 104, FC11 104, FC12 104 — GND
V15: +C15 475, +C16 475, +C17 475 — GND
VDDRREF: +C45 475 — GND
VDDRREF: FC73 104, FC74 104 — GND

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DSN:	
TITLE:	Altera Cyclone V F31 FPGA board
DOC. No:	ACM-028 B
FILE:	DDR.SchDoc
DATE:	2017/01/24 10:29:25
Sheet:	6 / 8

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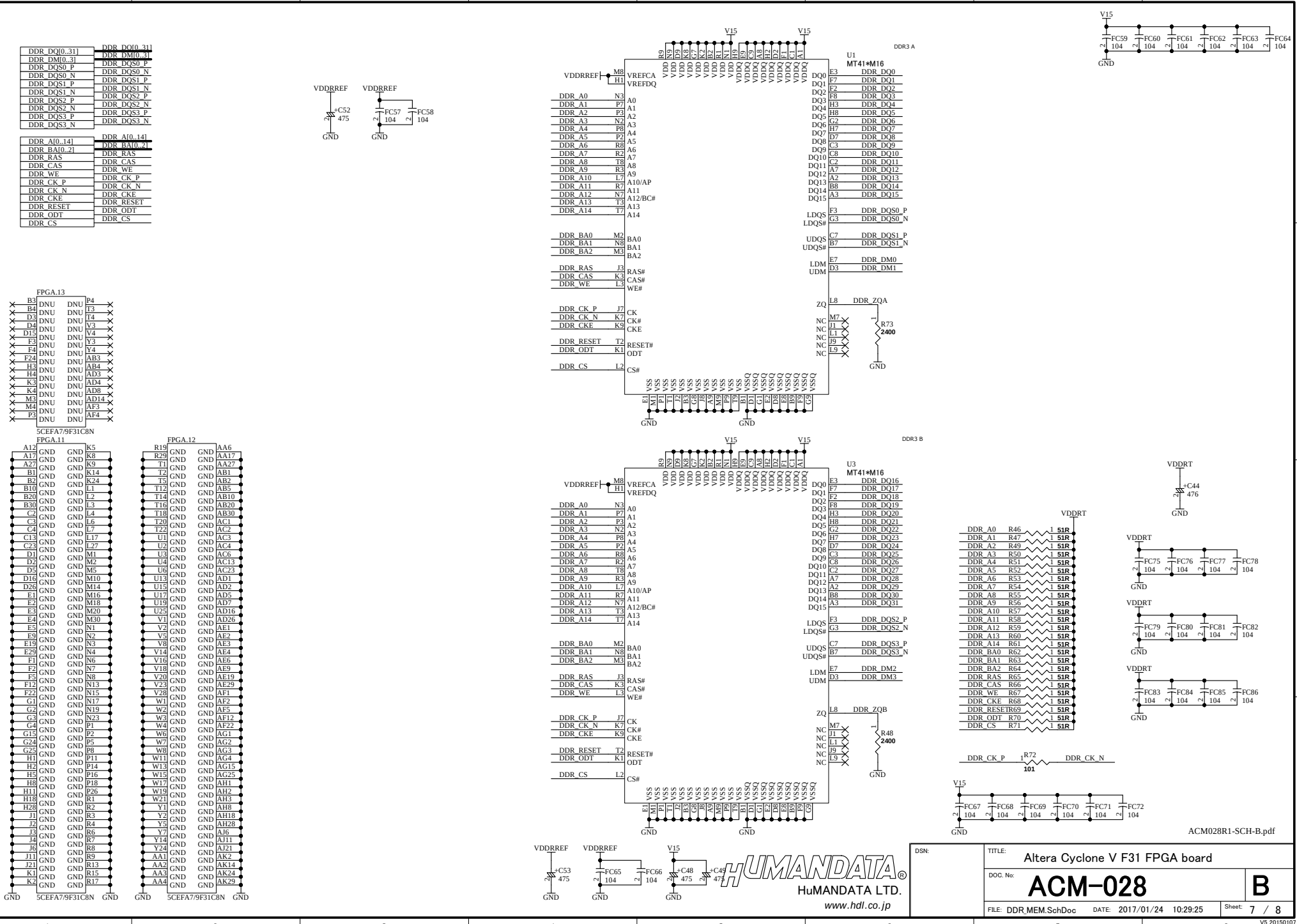
DDR_DQ[0..31]
DDR_DM[0..3]
DDR_DQS0_P
DDR_DQS0_N
DDR_DQS1_P
DDR_DQS1_N
DDR_DQS2_P
DDR_DQS2_N
DDR_DQS3_P
DDR_DQS3_N
DDR_A[0..14]
DDR_BA[0..2]
DDR_RAS
DDR_CAS
DDR_WE
DDR_CK_P
DDR_CK_N
DDR_CKE
DDR_RESET
DDR_ODT
DDR_CS
VDDRREF
+C52 475
FC57 104
FC58 104
GND
V15
U1
MT41*M16
DDR3 A
VREFCA
VREFDQ
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
LDQS
LDQS#
UDQS
UDQS#
LDM
UDM
ZQ
DDR_ZQA
R73 2400
NC
VSS
VSSQ
FC59 104
FC60 104
FC61 104
FC62 104
FC63 104
FC64 104
FPGA.13
5CEFA7/9F31C8N
FPGA.11
FPGA.12
U3
DDR3 B
DDR_ZQB
R48 2400
+C44 476
VDDRT
FC75 104
FC76 104
FC77 104
FC78 104
FC79 104
FC80 104
FC81 104
FC82 104
FC83 104
FC84 104
FC85 104
FC86 104
R46 51R
R47 51R
R49 51R
R50 51R
R51 51R
R52 51R
R53 51R
R54 51R
R55 51R
R56 51R
R57 51R
R58 51R
R59 51R
R60 51R
R61 51R
R62 51R
R63 51R
R64 51R
R65 51R
R66 51R
R67 51R
R68 51R
R69 51R
R70 51R
R71 51R
DDR_CK_P
R72 101
DDR_CK_N
FC67 104
FC68 104
FC69 104
FC70 104
FC71 104
FC72 104
+C53 475
FC65 104
FC66 104
+C48 475
+C49 475
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DSN:
TITLE:
Altera Cyclone V F31 FPGA board
DOC. No:
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FILE: DDR_MEM.SchDoc
DATE: 2017/01/24 10:29:25
Sheet: 7 / 8
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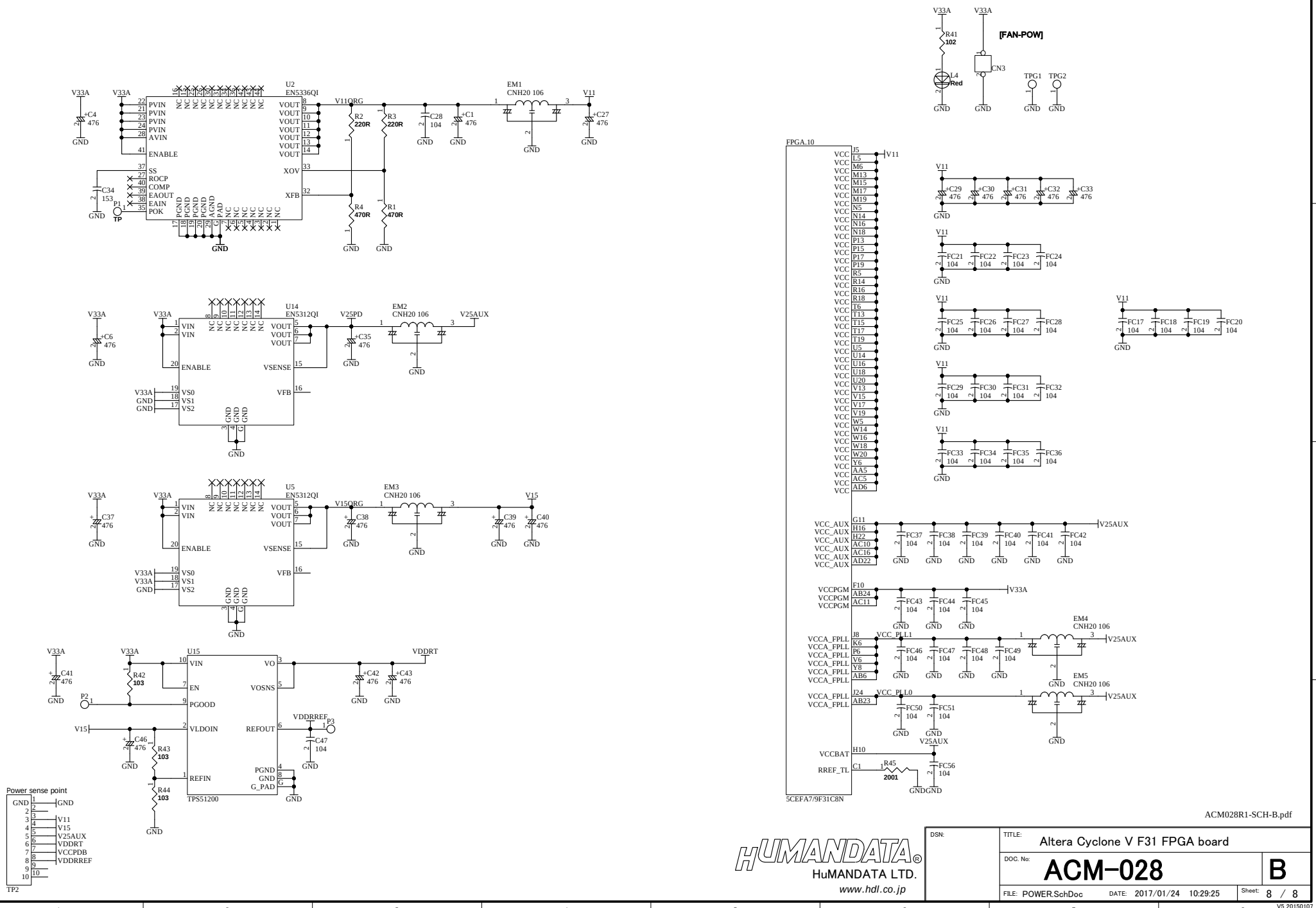

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DSN:	TITLE: Altera Cyclone V F31 FPGA board	
	DOC. No: ACM-028	B
	FILE: POWER.SchDoc DATE: 2017/01/24 10:29:25	Sheet: 8 / 8

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