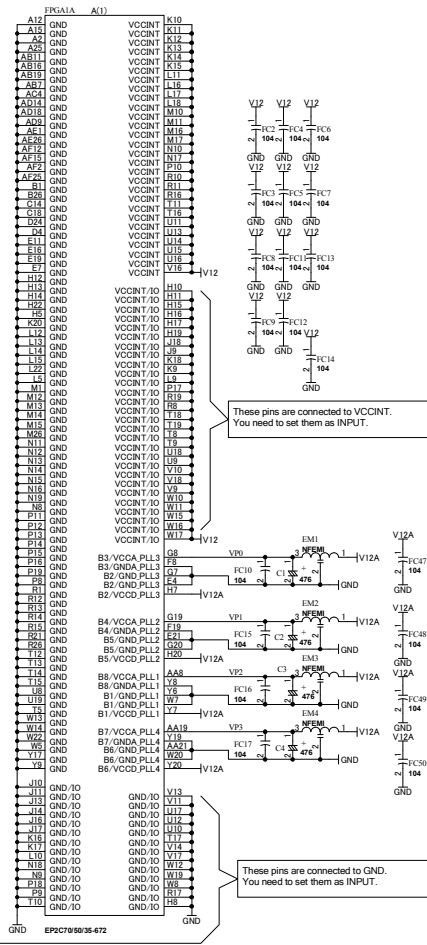
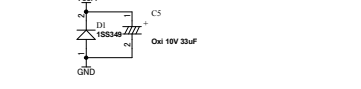
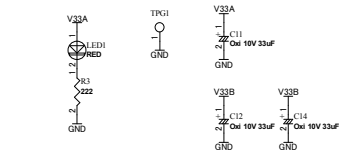
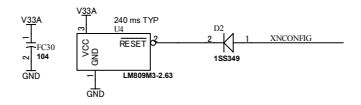
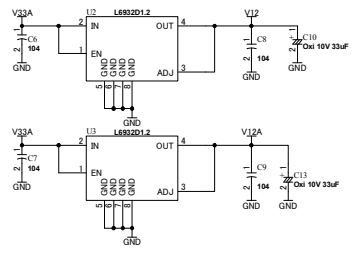


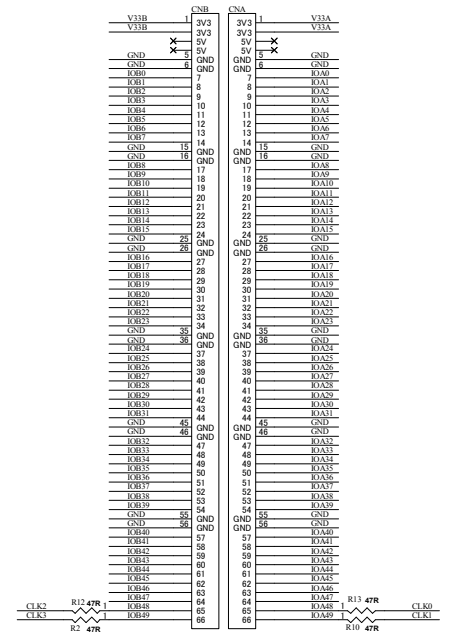
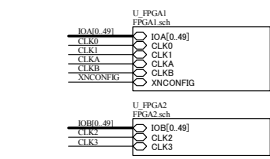
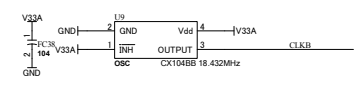
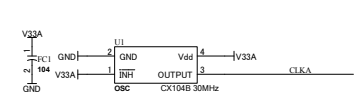
V12
V12A
V33A
V33B

GND GND

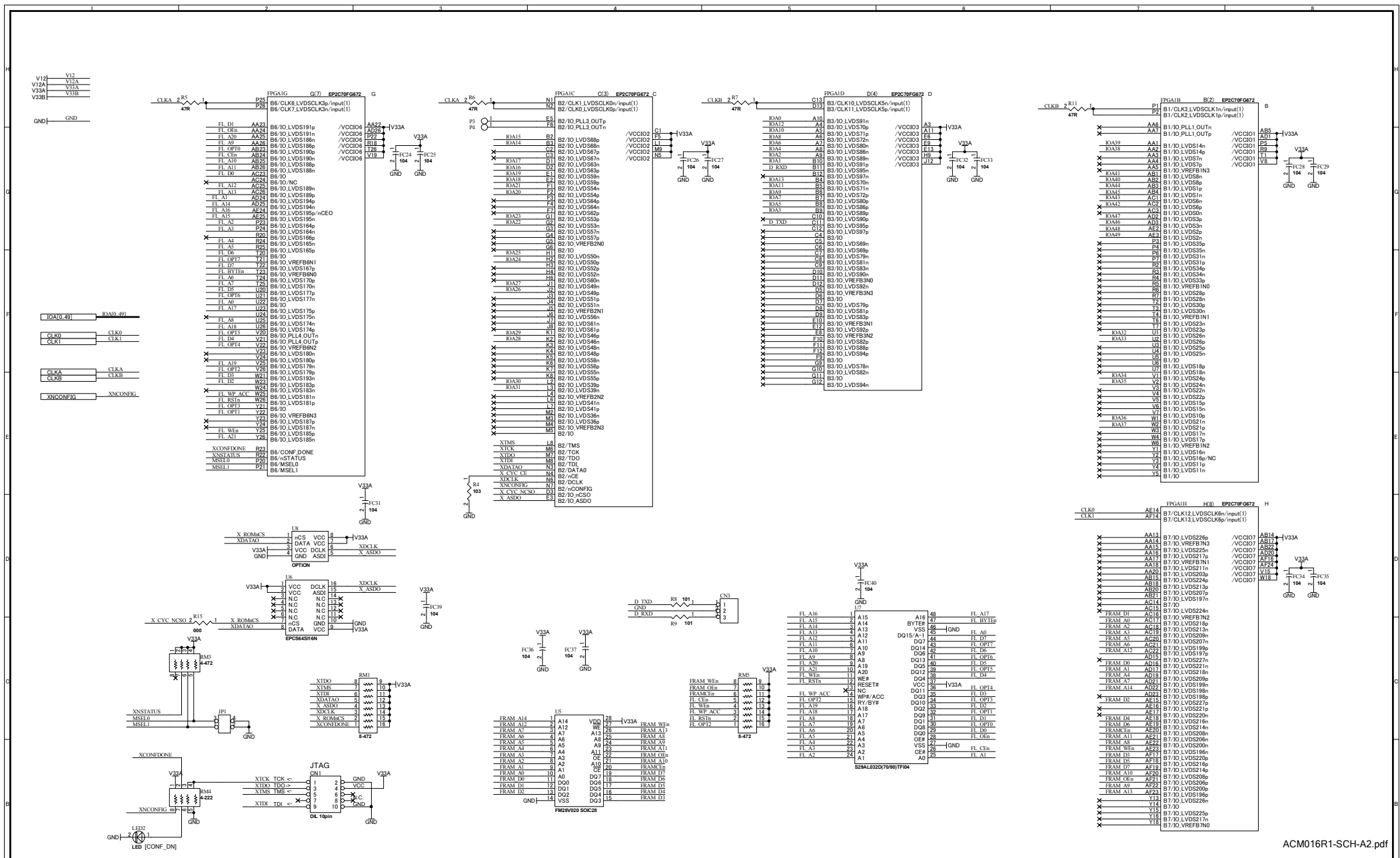


These pins are connected to VCCINT. You need to set them as INPUT.

These pins are connected to GND. You need to set them as INPUT.



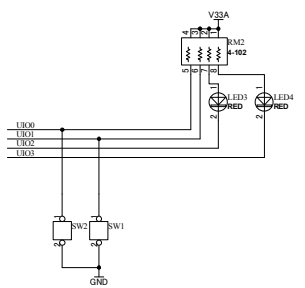
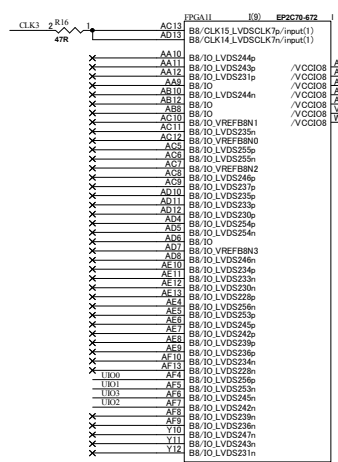
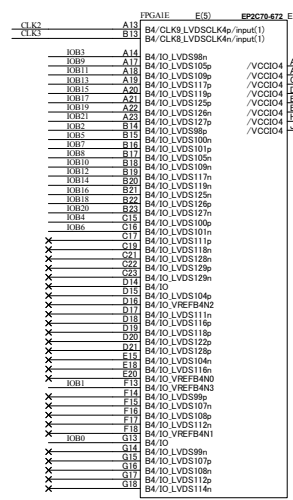
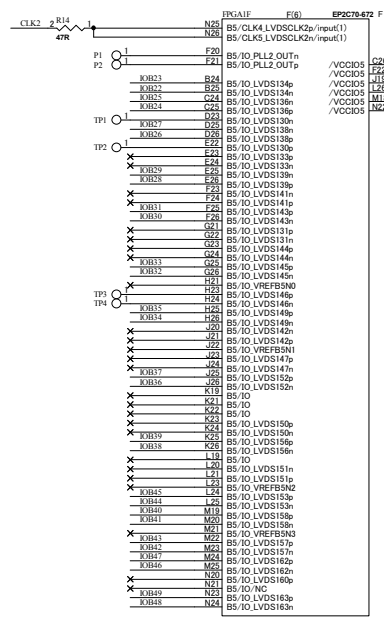
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V12 V12
V12A V12A
V33A V33A
V33B V33B
GND GND

ROBI(0..49) ROBI0..49
CLK2 CLK2
CLK3 CLK3



	2010/12/13	-----		Altera CycloneII F672 FPGA board	DOC. No. ACM-016	A2
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