

ACM-014-XX SRAM 設定例

Interface to User Logic - ext_ram

Ports | Instantiation | Timing | Publish

Bus Interface Type: Avalon Memory Slave

Design Files

Import Verilog, VHDL, EDIF, or Quartus Schematic File

Add... Delete

Top module:

Port Information

Port Name	Width	Direction	Shared	Type
ads	15	input	<input type="checkbox"/>	address
db	8	input	<input checked="" type="checkbox"/>	data
oen	1	input	<input type="checkbox"/>	outputenable_n
cen	1	input	<input checked="" type="checkbox"/>	chipselect_n
wen	1	input	<input type="checkbox"/>	write_n

Add generic list of ports Add Port Delete Port

Hide Advanced Signal Types

AHB Slave's Addressable Space

Address span: 0x100000000 Bits: 32

Cancel < Prev Next > Finish Editing Add to Library

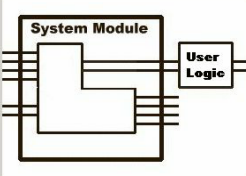
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Do not simulate user logic (An empty module will be inserted instead).

Simulate user logic (Imported HDL will be simulated with the system).

Export Bus Ports (You must manually connect every port correctly).



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Setup: 2 Wait: 2 Hold: 2 Units: Cycles

System Clock 30 MHz Timing granularity is System Clock cycles.

Read Waveforms

data addr select readn 1.9799999999999999 1.9799999999999999 cycles

Write Waveforms

data addr select writen 1.9799999999999999 1.9799999999999999 cycles 1.9799999999999999 1.9799999999999999 cyc

Cancel < Prev Next > Finish Editing Add to Library