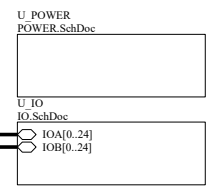


[DONE]

FPGA	
GCLK50_L	E2 CLK0_DIFFCLK_0p/B1
GND	E1 CLK1_DIFFCLK_0n/B1
XASDO	C2 IO_DIFFIO_L3p/B1
X_NCSO	C1 IO_DATA_LASDO_DIFFIO_L3n/B1
	D2 IO_FLASH_nCE_nCSO_DIFFIO_L4p/B1
	D1 IO_DIFFIO_L4n/B1
XTCK	H3 TCK/B1
XTDO	J4 TDO/B1
XTMS	J5 TMS/B1
XTDI	H4 TDI/B1
XNSTATUS	F4 nSTATUS/B1
XDCLK	H1 IO_DCLK/B1
XDATA	H2 IO_DATA0/B1
XNCONFIG	H5 nCONFIG/B1
GND	J3 nCE/B1
	B1 IO/B1(IO006/010/016)
	G2 IO_DIFFIO_L6p/B1(IO006/010/016)
	F3 IO_VREFB1N0/B1
	G1 IO_DIFFIO_L6n/B1(IO_VREFB1N1(016))(IO006/010)
V33P	E3 VCCIO1
	G3 VCCIO1
	U256 CY10 U256
	FPGAH
GCLK50_R	E16 CLK5_DIFFCLK_2n/B6
	E15 CLK4_DIFFCLK_2p/B6
ULED2	F15 IO_CLKUSR_DIFFIO_R4p/B6
	C16 IO_DIFFIO_R1n/B6
	C15 IO_DIFFIO_R1p/B6
XNCONDONE	H14 CONF_DONE/B6
GND	H13 MSEL0/B6
MSEL	H12 MSEL1/B6
GND	G12 MSEL2/B6
	G16 IO_INIT_DONE_DIFFIO_R5n/B6
	G15 IO_CRC_ERROR_DIFFIO_R5p/B6
	F16 IO_nCE0_DIFFIO_R4n/B6
	B16 IO/B6(IO006/010/016)
	D16 IO/B6(IO006/010/016)
	D15 IO/B6(IO006/010/016)
DSW	F13 IO/B6(IO_VREFB6N1(016))(IO006/010)
ULED1	F14 IO_VREFB6N0/B6
V33P	E14 VCCIO6
	G14 VCCIO6
	U256 CY10 U256

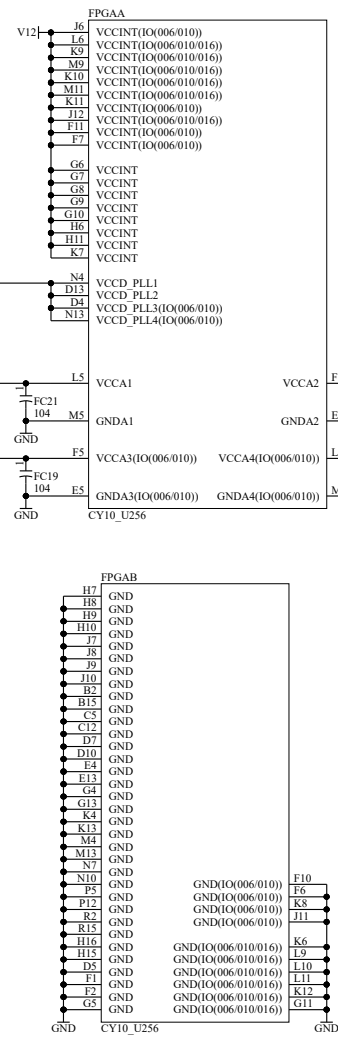
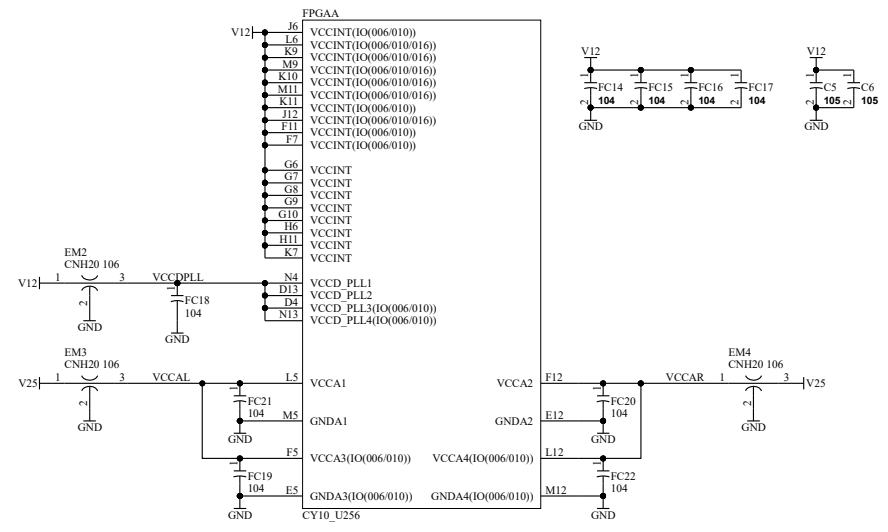
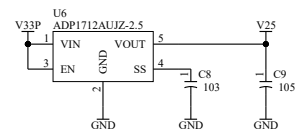
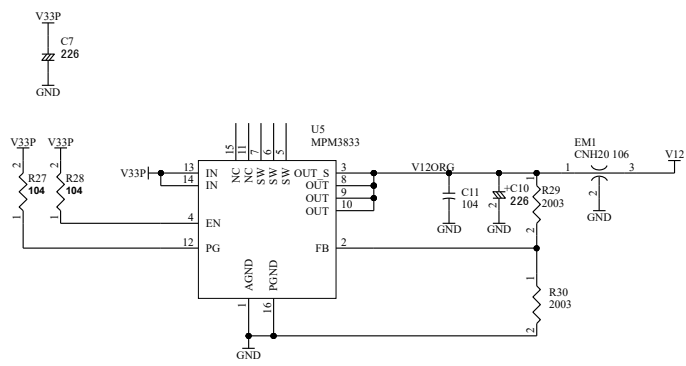
CN1		
IOB0	1 IOB/GCLKIOA/GCLK	68 IOA0
IOB1	2 IOB/GCLKIOA/GCLK	67 IOA1
IOB2	3 IOB	66 IOA2
IOB3	4 IOB	65 IOA3
IOB4	5 IOB	64 IOA4
IOB5	6 IOB	63 IOA5
IOB6	7 IOB	62
IOB7	8 IOB	61 VIOA
	9 IOB	60 GND
	10 GND	59 GND
	11 GND	58 IOA6
IOB8	12 VIOB	57 IOA7
IOB9	13 IOB	56 IOA8
IOB10	14 IOB	55 IOA9
IOB11	15 IOB	54 IOA10
IOB12	16 IOB	53 IOA11
IOB13	17 IOB	52 IOA12
IOB14	18 IOB	51 IOA13
IOB15	19 IOB	50 IOA14
IOB16	20 IOB	49 IOA15
IOB17	21 IOB	48 IOA16
IOB18	22 IOB	47 IOA17
IOB19	23 IOB	46 IOA18
IOB20	24 IOB	45 IOA19
IOB21	25 IOB	44 VIOA
	26 IOB	43 GND
	27 GND	42 GND
	28 GND	41 IOA20
IOB22	29 VIOB	40 IOA21
IOB23	30 IOB	39 IOA22
IOB24	31 IOB	38 IOA23
		37 IOA24
		36 TCK
		35 TDO
		34 TMS
		33 TDI
		32 PLCC68



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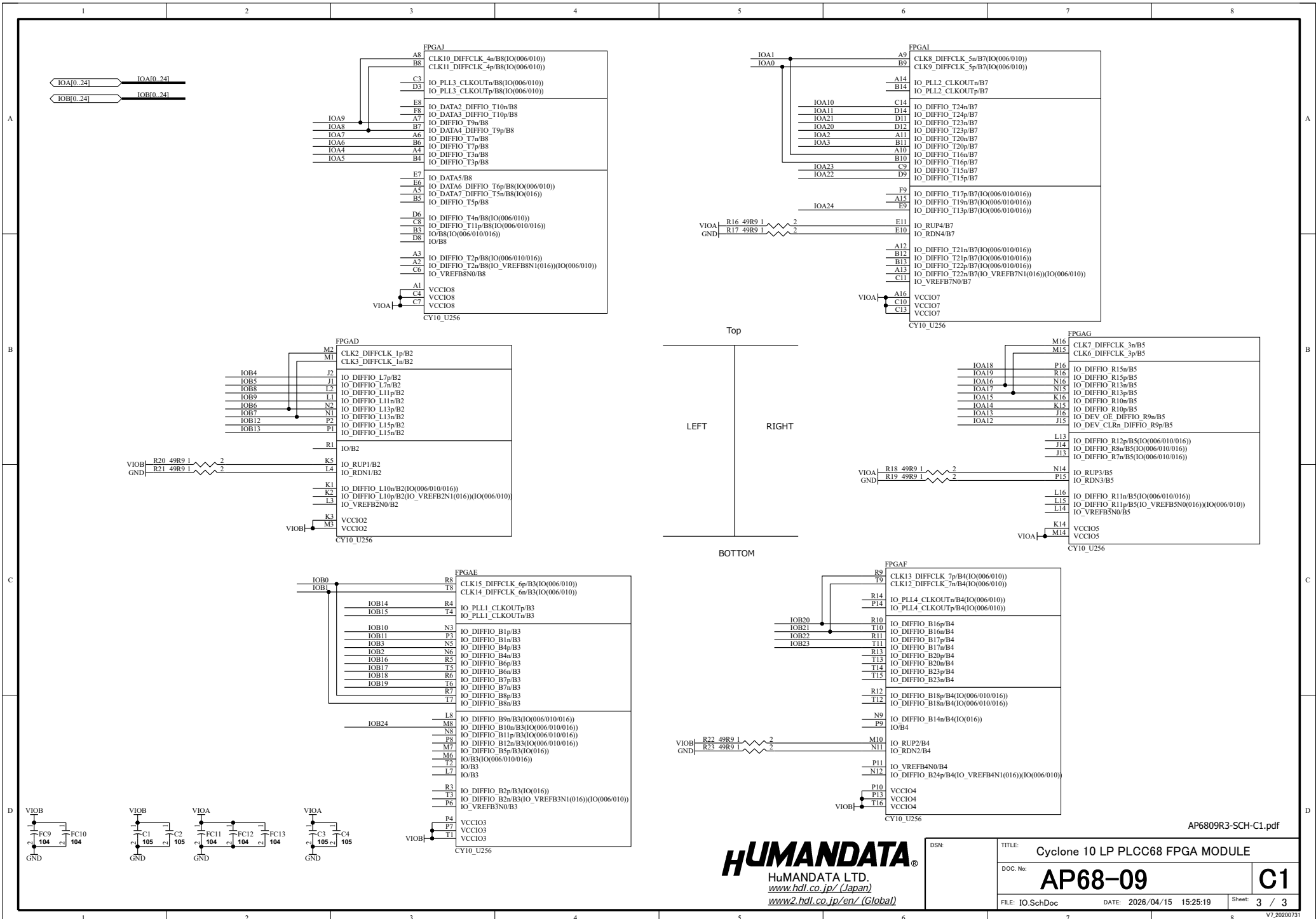
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