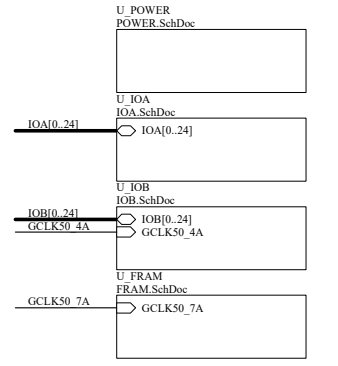
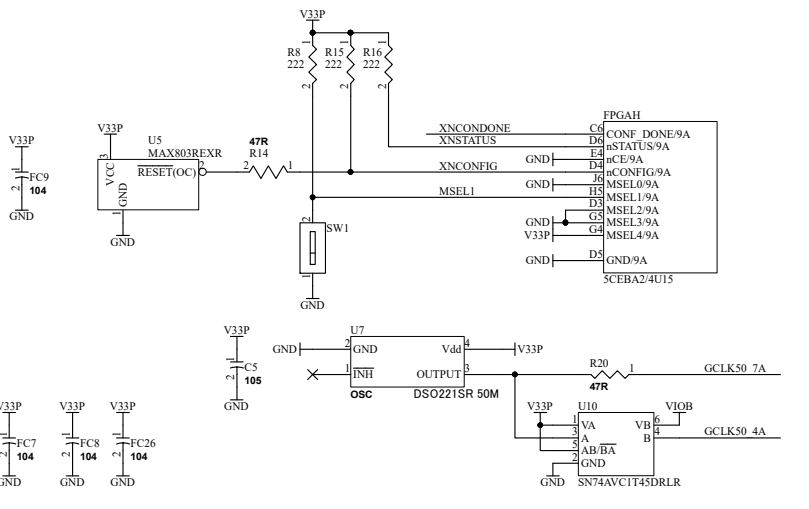
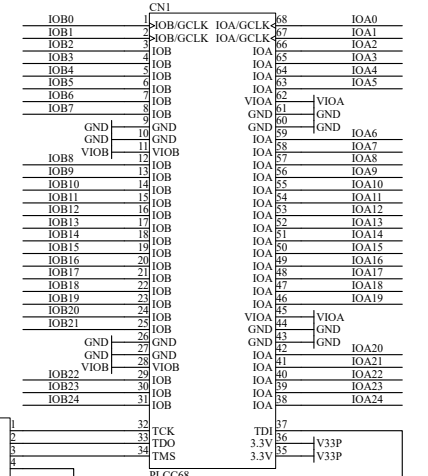
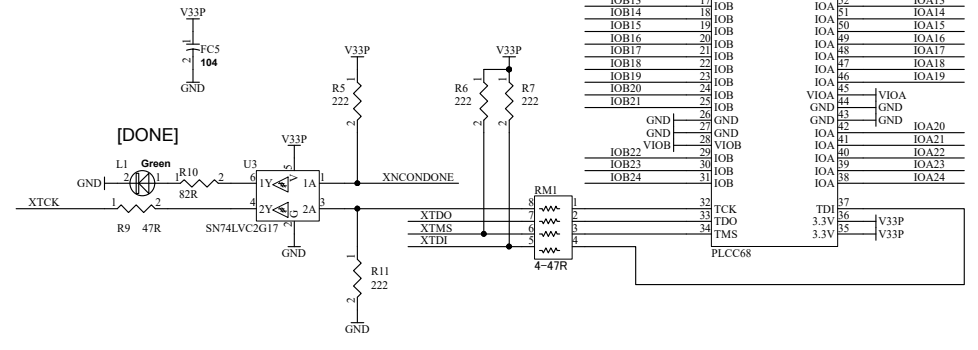
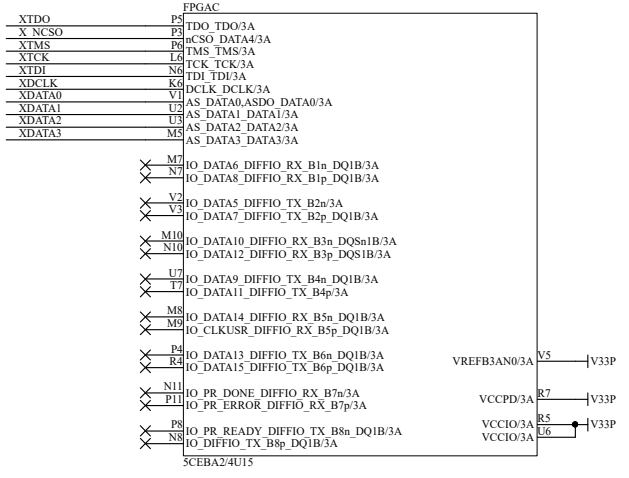
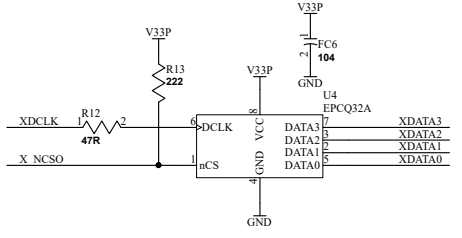
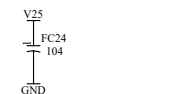
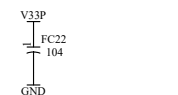
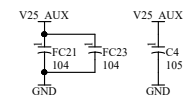
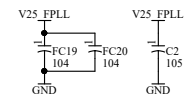
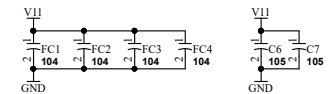
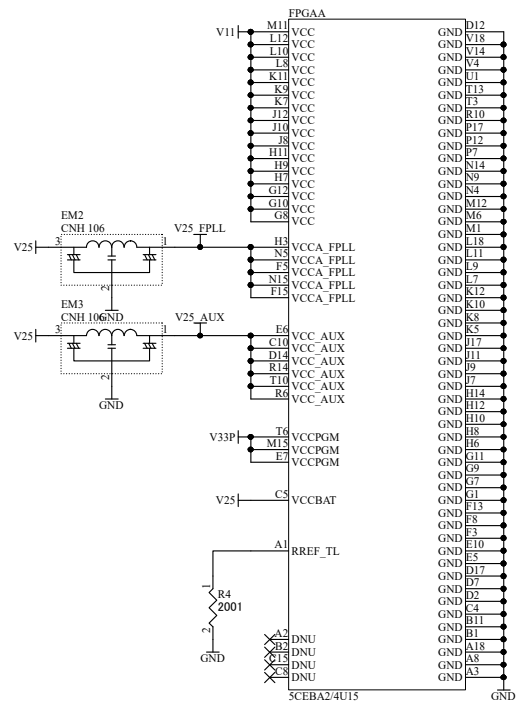
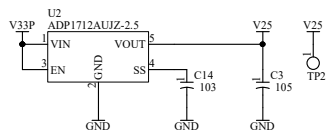
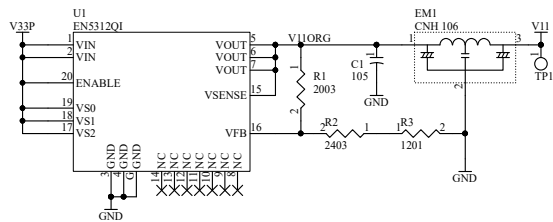


A  
B  
C  
D



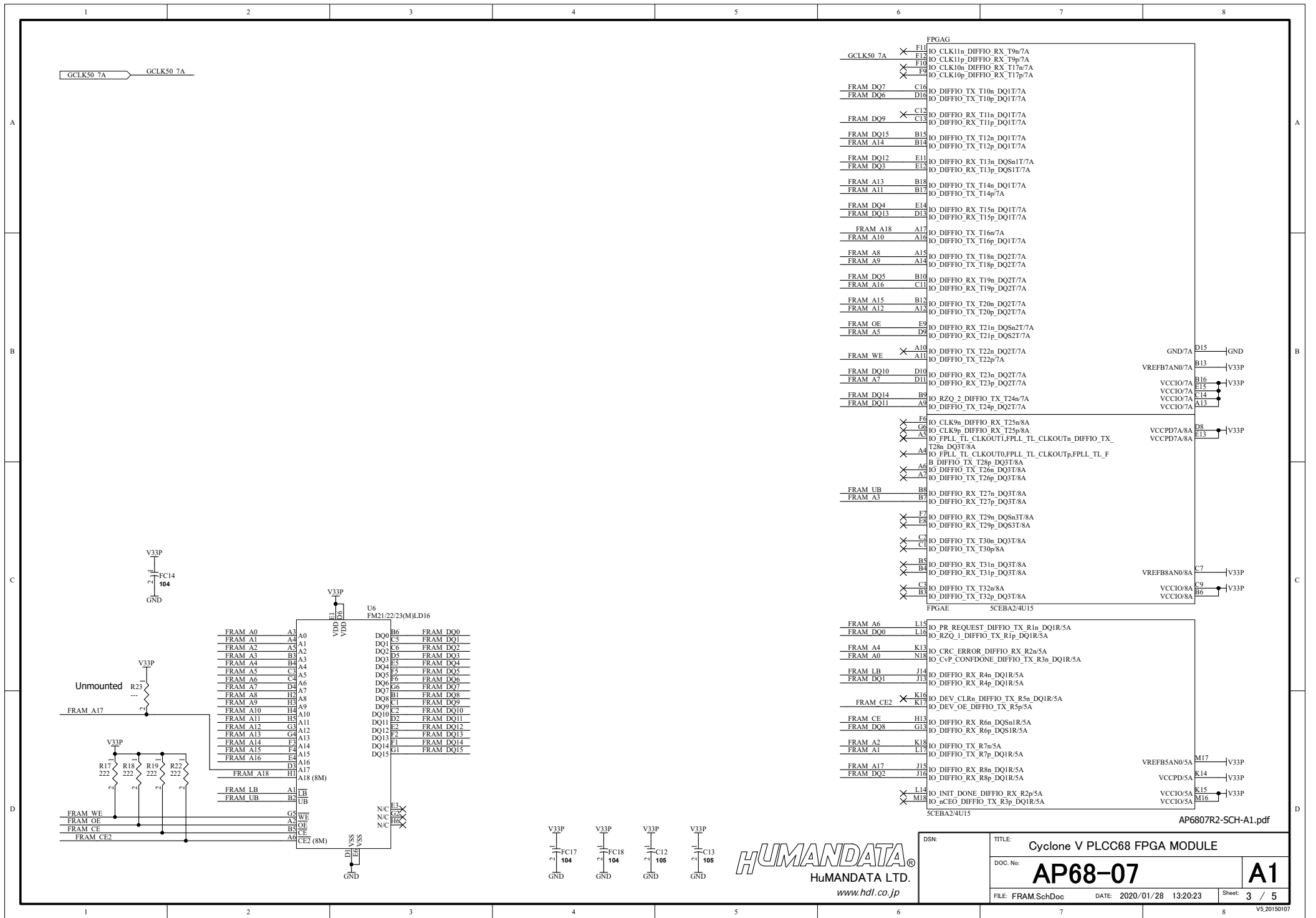
DSN:	TITLE: Cyclone V PLCC68 FPGA MODULE
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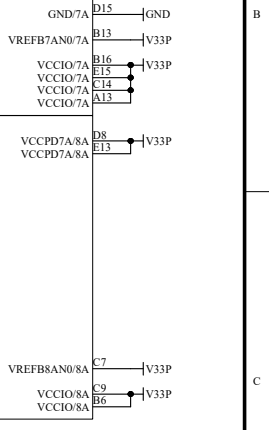


DSN:	TITLE: Cyclone V PLCC68 FPGA MODULE	<b>A1</b>
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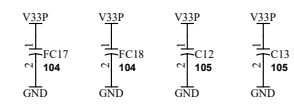
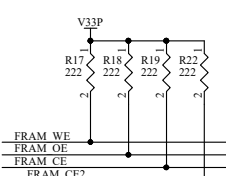
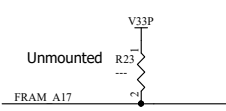
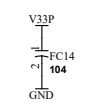


Pin	Signal	Internal Pin	Internal Signal	External Pin	External Signal
GCLK50 7A	F11	F11	IO_CLK11n_DIFFIO_RX_T9n/7A		
	F12	F12	IO_CLK11p_DIFFIO_RX_T9p/7A		
	F10	F10	IO_CLK10n_DIFFIO_RX_T17n/7A		
	F9	F9	IO_CLK10p_DIFFIO_RX_T17p/7A		
FRAM D07	C16	C16	IO_DIFFIO_TX_T10n_DQ17/7A		
FRAM D06	D16	D16	IO_DIFFIO_TX_T10p_DQ17/7A		
FRAM D09	C12	C13	IO_DIFFIO_RX_T11n_DQ17/7A		
	C13	C13	IO_DIFFIO_RX_T11p_DQ17/7A		
FRAM DQ15	B15	B15	IO_DIFFIO_TX_T12n_DQ17/7A		
FRAM A14	B14	B14	IO_DIFFIO_TX_T12p_DQ17/7A		
FRAM DQ12	E11	E11	IO_DIFFIO_RX_T13n_DQ8n17/7A		
FRAM DQ3	E12	E12	IO_DIFFIO_RX_T13p_DQ8n17/7A		
FRAM A13	B18	B18	IO_DIFFIO_TX_T14n_DQ17/7A		
FRAM A11	B17	B17	IO_DIFFIO_TX_T14p_7A		
FRAM DQ4	E14	E14	IO_DIFFIO_RX_T15n_DQ17/7A		
FRAM DQ13	D13	D13	IO_DIFFIO_RX_T15p_DQ17/7A		
FRAM A18	A17	A17	IO_DIFFIO_TX_T16n_7A		
FRAM A10	A16	A16	IO_DIFFIO_TX_T16p_DQ17/7A		
FRAM A8	A15	A15	IO_DIFFIO_TX_T18n_DQ27/7A		
FRAM A9	A14	A14	IO_DIFFIO_TX_T18p_DQ27/7A		
FRAM DQ5	B10	B10	IO_DIFFIO_RX_T19n_DQ27/7A		
FRAM A16	C11	C11	IO_DIFFIO_RX_T19p_DQ27/7A		
FRAM A15	B12	B12	IO_DIFFIO_TX_T20n_DQ27/7A		
FRAM A12	A12	A12	IO_DIFFIO_TX_T20p_DQ27/7A		
FRAM OE	E9	E9	IO_DIFFIO_RX_T21n_DQ8n27/7A		
FRAM A5	D9	D9	IO_DIFFIO_RX_T21p_DQ8n27/7A		
FRAM WE	A10	A11	IO_DIFFIO_TX_T22n_DQ27/7A		
	A11	A11	IO_DIFFIO_TX_T22p_7A		
FRAM DQ10	D10	D10	IO_DIFFIO_RX_T23n_DQ27/7A		
FRAM A7	D11	D11	IO_DIFFIO_RX_T23p_DQ27/7A		
FRAM DQ14	B9	B9	IO_RZQ_2_DIFFIO_TX_T24n/7A		
FRAM DQ11	A9	A9	IO_DIFFIO_TX_T24p_DQ27/7A		
	F6	F6	IO_CLK9n_DIFFIO_RX_T25n/8A		
	G6	G6	IO_CLK9p_DIFFIO_RX_T25p/8A		
	A5	A5	IO_FLL_TL_CLKOUT1,FPLL_TL_CLKOUTn_DIFFIO_TX_T28n_DQ37/8A		
	A4	A4	IO_FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_F		
	A6	A6	B_DIFFIO_TX_T28p_DQ37/8A		
	A7	A7	IO_DIFFIO_TX_T26n_DQ37/8A		
	A7	A7	IO_DIFFIO_TX_T26p_DQ37/8A		
FRAM UB	B8	B8	IO_DIFFIO_RX_T27n_DQ37/8A		
FRAM A3	B7	B7	IO_DIFFIO_RX_T27p_DQ37/8A		
	F7	F7	IO_DIFFIO_RX_T29n_DQ8n37/8A		
	E8	E8	IO_DIFFIO_RX_T29p_DQ8n37/8A		
	C2	C2	IO_DIFFIO_TX_T30n_DQ37/8A		
	C1	C1	IO_DIFFIO_TX_T30p_8A		
	B5	B5	IO_DIFFIO_RX_T31n_DQ37/8A		
	B4	B4	IO_DIFFIO_RX_T31p_DQ37/8A		
	C3	C3	IO_DIFFIO_TX_T32n_8A		
	B3	B3	IO_DIFFIO_TX_T32p_DQ37/8A		

Pin	Signal	Internal Pin	Internal Signal	External Pin	External Signal
FRAM A6	L15	L15	IO_PR_REQUEST_DIFFIO_TX_R1n_DQ1R/5A		
FRAM DQ0	L16	L16	IO_RZQ_1_DIFFIO_TX_R1p_DQ1R/5A		
FRAM A4	K13	K13	IO_CRC_ERROR_DIFFIO_RX_R2n/5A		
FRAM A0	N18	N18	IO_CvP_CONFEDONE_DIFFIO_TX_R3n_DQ1R/5A		
FRAM LB	J14	J14	IO_DIFFIO_RX_R4n_DQ1R/5A		
FRAM DQ1	J15	J15	IO_DIFFIO_RX_R4p_DQ1R/5A		
FRAM CE2	K16	K17	IO_DEV_CLKRn_DIFFIO_TX_R5n_DQ1R/5A		
	K17	K17	IO_DEV_OE_DIFFIO_TX_R5p/5A		
FRAM CE	H13	H13	IO_DIFFIO_RX_R6n_DQ8n1R/5A		
FRAM DQ8	G13	G13	IO_DIFFIO_RX_R6p_DQ8n1R/5A		
FRAM A2	K18	K18	IO_DIFFIO_TX_R7n/5A		
FRAM A1	L17	L17	IO_DIFFIO_TX_R7p_DQ1R/5A		
FRAM A17	J15	J15	IO_DIFFIO_RX_R8n_DQ1R/5A		
FRAM DQ2	J16	J16	IO_DIFFIO_RX_R8p_DQ1R/5A		
	L14	L14	IO_INIT_DONE_DIFFIO_RX_R2p/5A		
	M18	M18	IO_nCEO_DIFFIO_TX_R3p_DQ1R/5A		

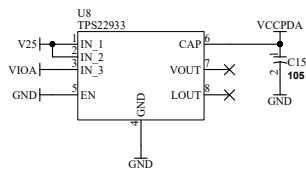
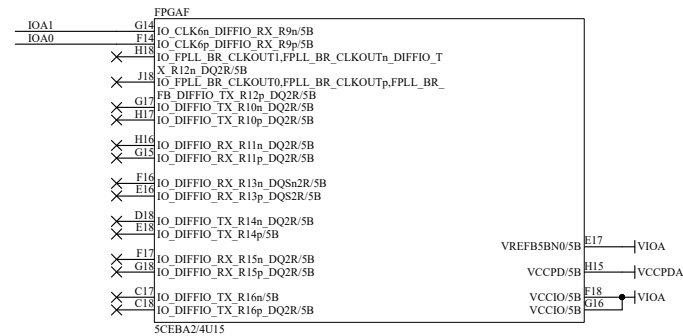
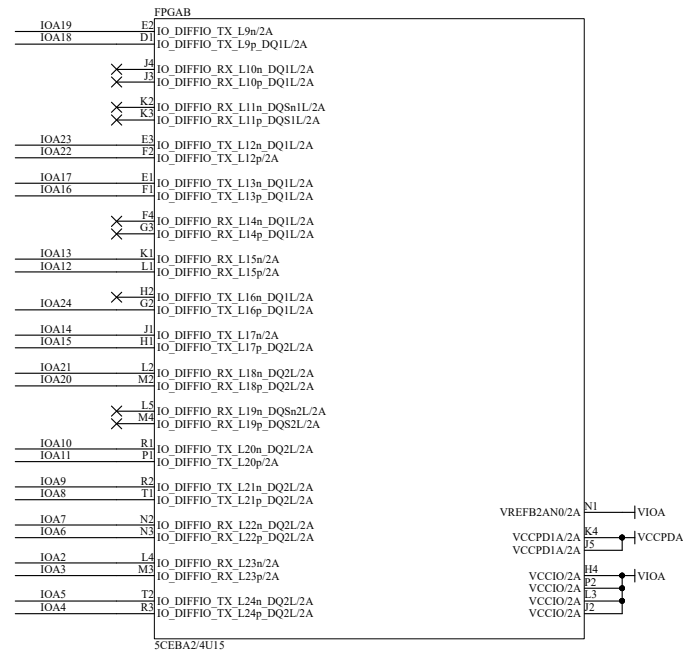


GCLK50 7A



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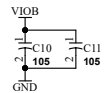
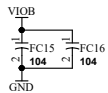
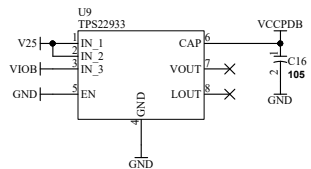
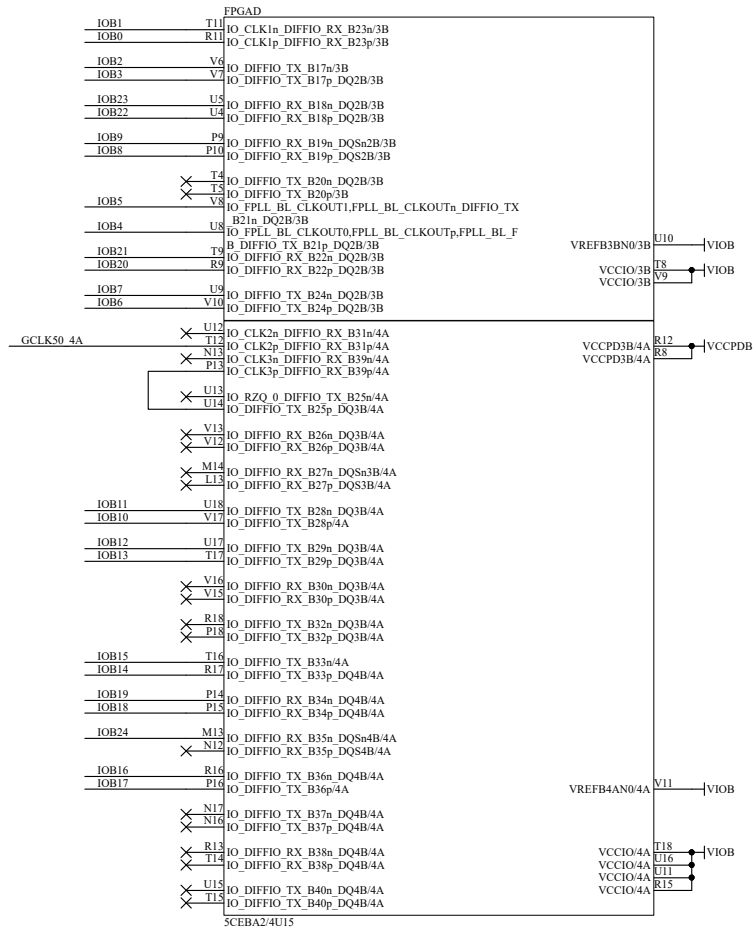
IOA[0..24]



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DSN:	TITLE: Cyclone V PLCC68 FPGA MODULE
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