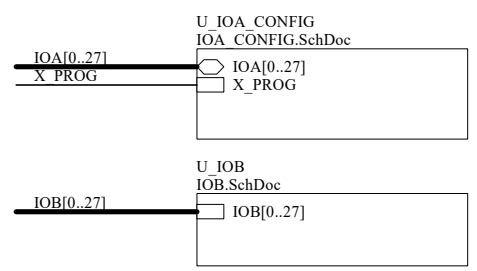
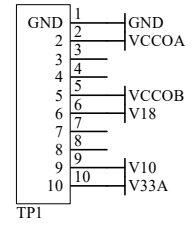
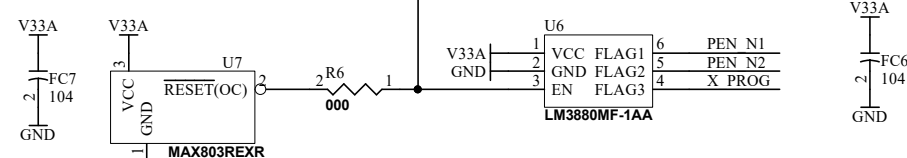
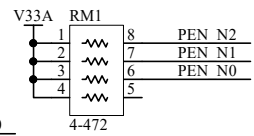
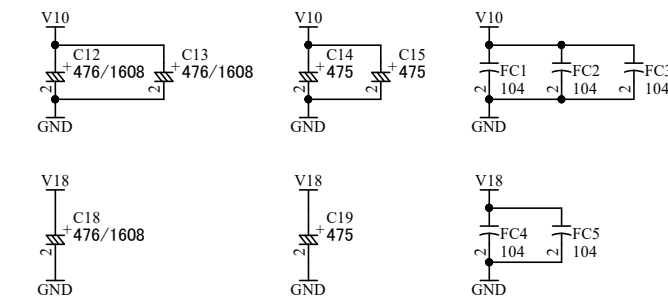
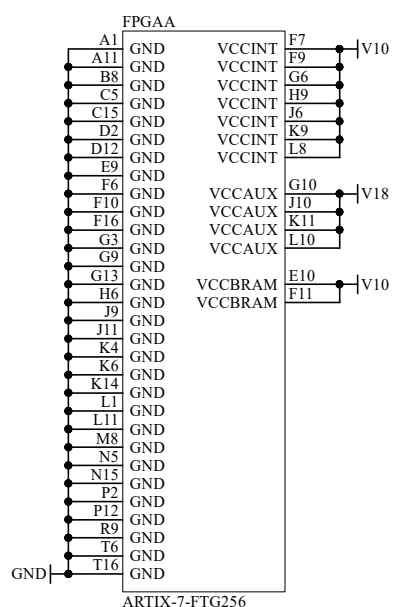
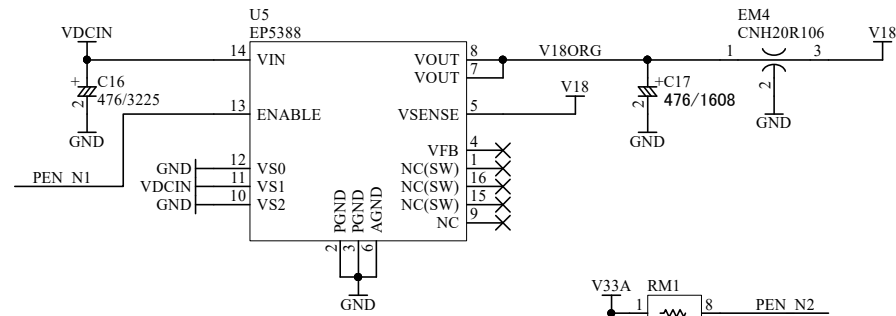
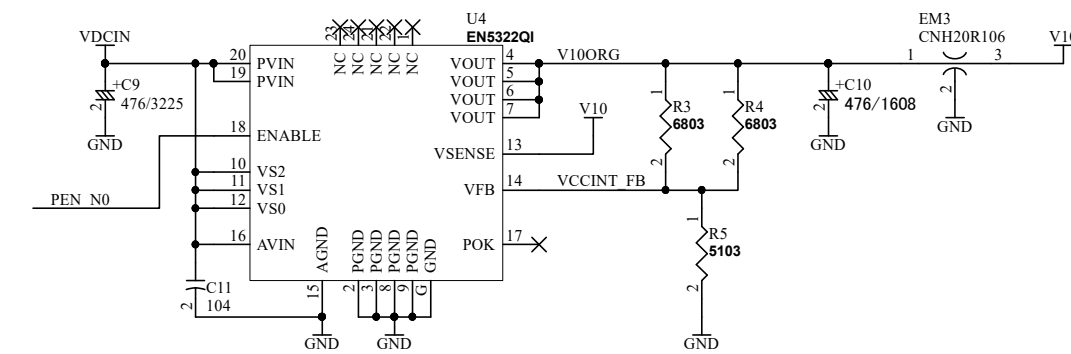
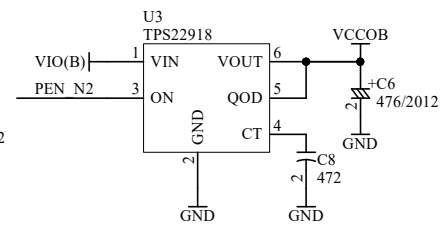
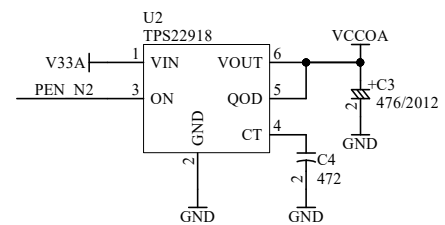
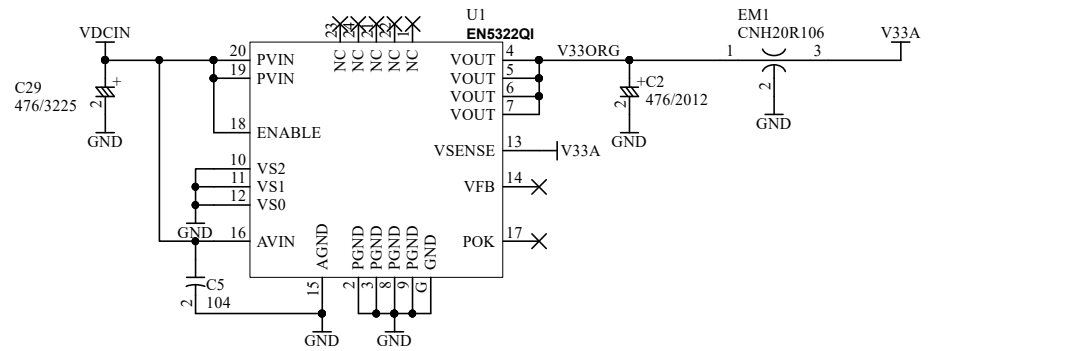
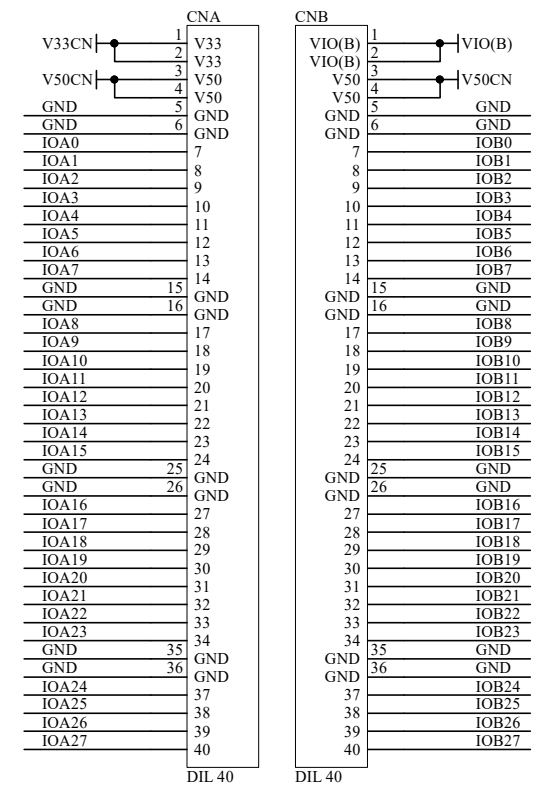
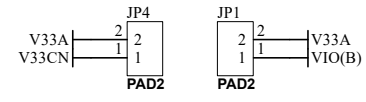
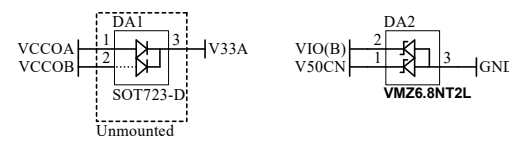
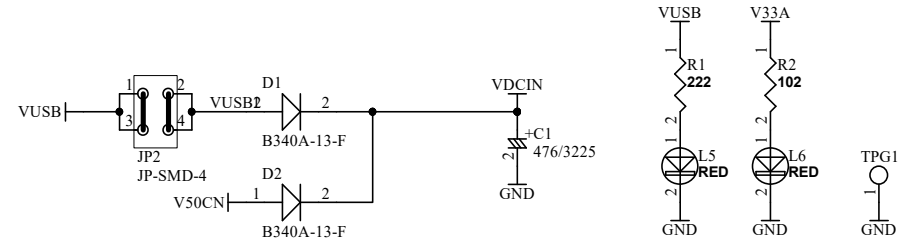
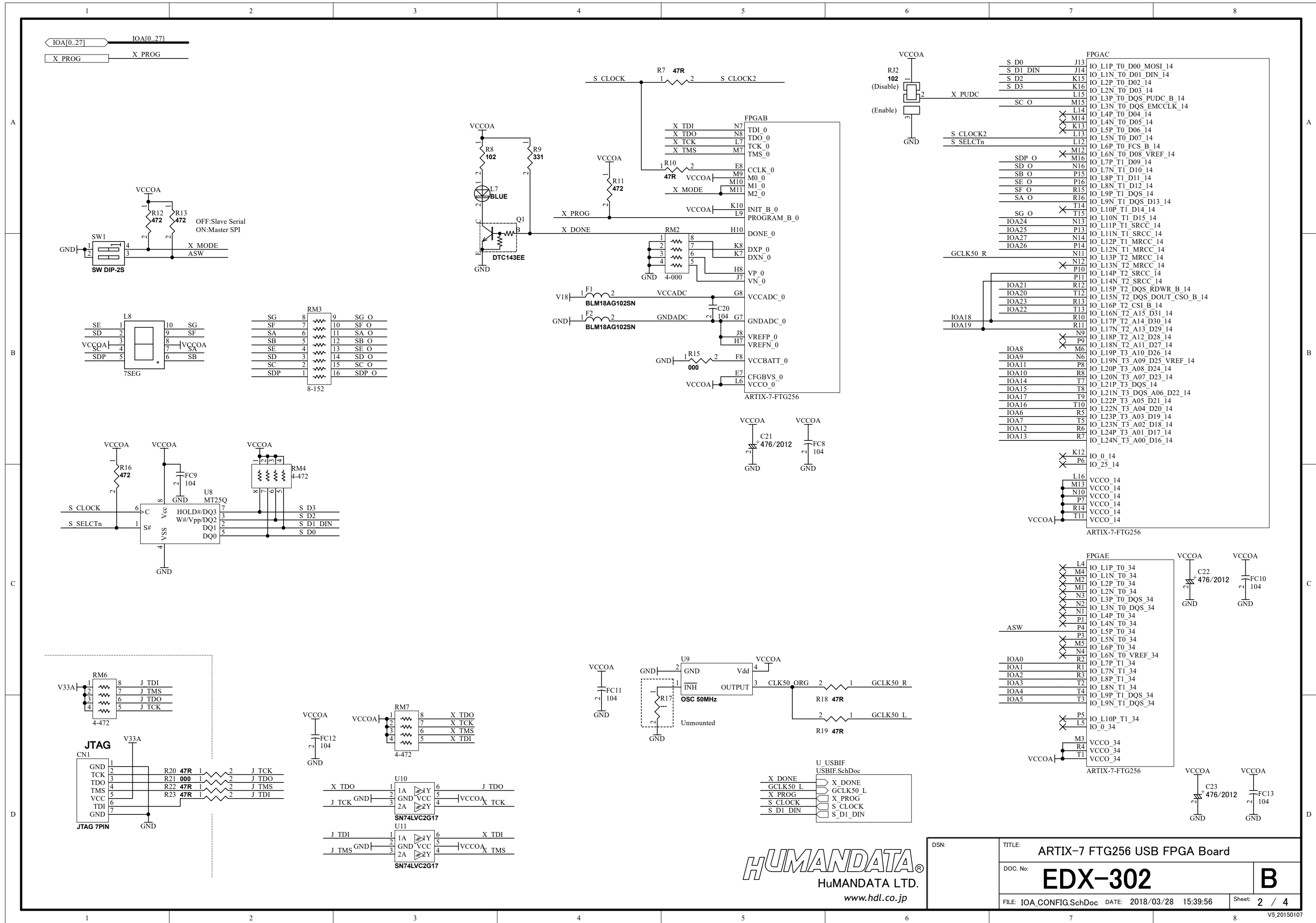


[POWER]



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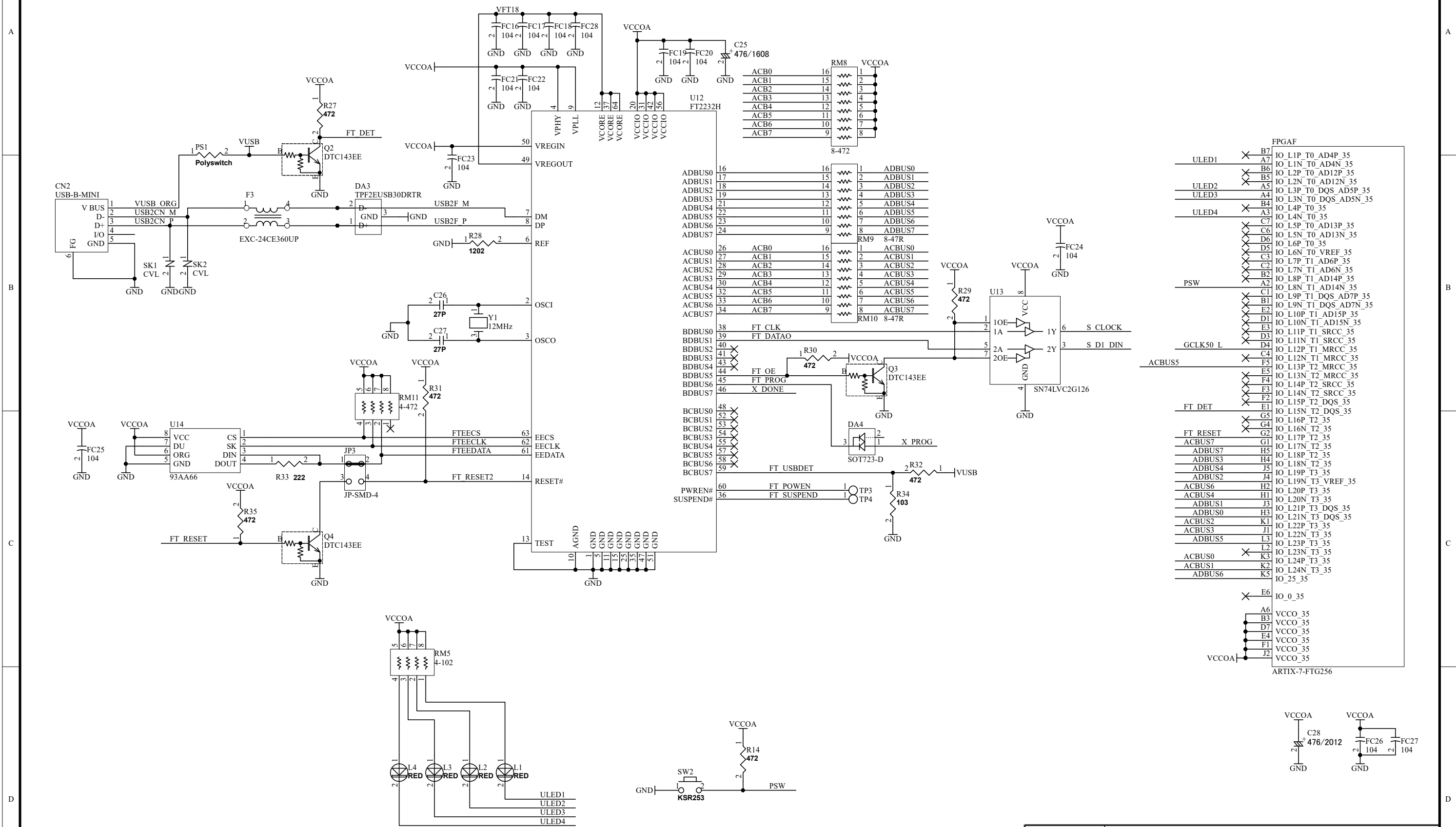
DSN:	TITLE: ARTIX-7 FTG256 USB FPGA Board
DOC. No: EDX-302	B
FILE: EDX302B.sch	DATE: 2018/03/28 15:39:55
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GCLK50 L  
 S CLOCK  
 S DI DIN  
 X PROG  
 X DONE



FPGA

IO L1P_T0_AD4P_35	B7
IO L1N_T0_AD4N_35	A7
IO L2P_T0_AD12P_35	B5
IO L2N_T0_AD12N_35	A5
IO L3P_T0_DQS_AD5P_35	A4
IO L3N_T0_DQS_AD5N_35	B4
IO L4P_T0_35	A3
IO L4N_T0_35	B3
IO L5P_T0_AD13P_35	C7
IO L5N_T0_AD13N_35	C6
IO L6P_T0_35	D6
IO L6N_T0_VREF_35	D5
IO L7P_T1_AD6P_35	C3
IO L7N_T1_AD6N_35	C2
IO L8P_T1_AD14P_35	B2
IO L8N_T1_AD14N_35	A2
IO L9P_T1_DQS_AD7P_35	C1
IO L9N_T1_DQS_AD7N_35	B1
IO L10P_T1_AD15P_35	E2
IO L10N_T1_AD15N_35	E1
IO L11P_T1_SRCC_35	D3
IO L12P_T1_MRCC_35	D4
IO L12N_T1_MRCC_35	F5
IO L13P_T2_MRCC_35	E5
IO L13N_T2_MRCC_35	F4
IO L14P_T2_SRCC_35	F3
IO L14N_T2_SRCC_35	F2
IO L15P_T2_DQS_35	E1
IO L15N_T2_DQS_35	G5
IO L16P_T2_35	G4
IO L16N_T2_35	G1
IO L17P_T2_35	G1
IO L17N_T2_35	H5
IO L18P_T2_35	H4
IO L18N_T2_35	J5
IO L19P_T3_35	J4
IO L19N_T3_VREF_35	H2
IO L20P_T3_35	H1
IO L20N_T3_35	J3
IO L21P_T3_DQS_35	J3
IO L21N_T3_DQS_35	K1
IO L22P_T3_35	J1
IO L22N_T3_35	L3
IO L23P_T3_35	L3
IO L23N_T3_35	L2
IO L24P_T3_35	K3
IO L24N_T3_35	K2
IO_25_35	K5
IO_0_35	E6
VCCO_35	A6
VCCO_35	B3
VCCO_35	D7
VCCO_35	E4
VCCO_35	F1
VCCO_35	J2

ARTIX-7-FTG256

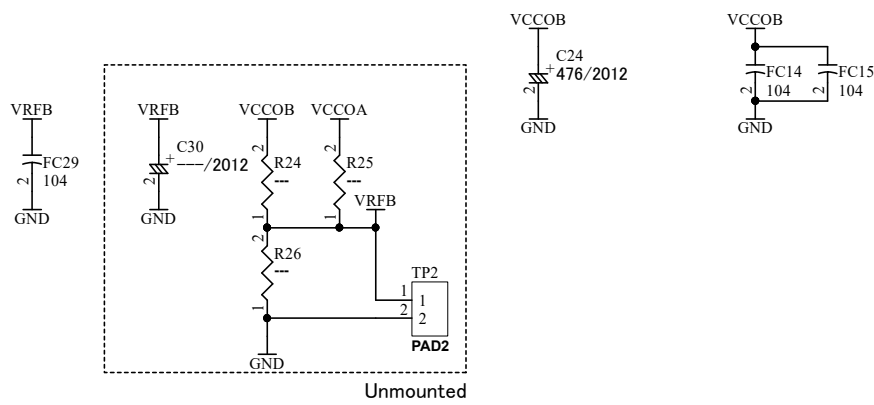
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DSN:	TITLE: ARTIX-7 FTG256 USB FPGA Board
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IOB[0..27]

IOB		FPGAD	
IOB0	C8	IO_L1P_T0_AD0P_15	
IOB1	C9	IO_L1N_T0_AD0N_15	
IOB17	A8	IO_L2P_T0_AD8P_15	
IOB16	A9	IO_L2N_T0_AD8N_15	
IOB19	B9	IO_L3P_T0_DQS_AD1P_15	
IOB18	A10	IO_L3N_T0_DQS_AD1N_15	
IOB8	B10	IO_L4P_T0_15	
IOB9	B11	IO_L4N_T0_15	
IOB22	B12	IO_L5P_T0_AD9P_15	
IOB23	A12	IO_L5N_T0_AD9N_15	
	D8	IO_L6P_T0_15	
	D9	IO_L6N_T0_VREF_15	
IOB25	VRFB	IO_L7P_T1_AD2P_15	
IOB24	A14	IO_L7N_T1_AD2N_15	
IOB12	C14	IO_L8P_T1_AD10P_15	
IOB13	B14	IO_L8N_T1_AD10N_15	
IOB26	B15	IO_L9P_T1_DQS_AD3P_15	
IOB27	A15	IO_L9N_T1_DQS_AD3N_15	
IOB20	C16	IO_L10P_T1_AD11P_15	
IOB21	B16	IO_L10N_T1_AD11N_15	
IOB6	C11	IO_L11P_T1_SRCC_15	
IOB7	C12	IO_L11N_T1_SRCC_15	
IOB10	D13	IO_L12P_T1_MRCC_15	
IOB11	C13	IO_L12N_T1_MRCC_15	
IOB4	E12	IO_L13P_T2_MRCC_15	
IOB5	E13	IO_L13N_T2_MRCC_15	
IOB3	E11	IO_L14P_T2_SRCC_15	
IOB2	D11	IO_L14N_T2_SRCC_15	
	D14	IO_L15P_T2_DQS_15	
	D15	IO_L15N_T2_DQS_ADV_B_15	
	F12	IO_L16P_T2_A28_15	
	F13	IO_L16N_T2_A27_15	
IOB14	E16	IO_L17P_T2_A26_15	
IOB15	D16	IO_L17N_T2_A25_15	
	F15	IO_L18P_T2_A24_15	
	E15	IO_L18N_T2_A23_15	
	H11	IO_L19P_T3_A22_15	
	G12	IO_L19N_T3_A21_VREF_15	
	H12	IO_L20P_T3_A20_15	
	H13	IO_L20N_T3_A19_15	
	G14	IO_L21P_T3_DQS_15	
	F14	IO_L21N_T3_DQS_A18_15	
	H16	IO_L22P_T3_A17_15	
	G16	IO_L22N_T3_A16_15	
	J15	IO_L23P_T3_FOE_B_15	
	J16	IO_L23N_T3_FWE_B_15	
	H14	IO_L24P_T3_RS1_15	
	G15	IO_L24N_T3_RS0_15	
	D10	IO_0_15	
	G11	IO_25_15	
	A16	VCCO_15	
	B13	VCCO_15	
	C10	VCCO_15	
	E14	VCCO_15	
	H15	VCCO_15	
VCCOB	J12	VCCO_15	

ARTIX-7-FTG256



Unmounted



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