


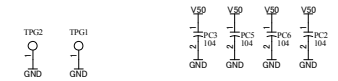
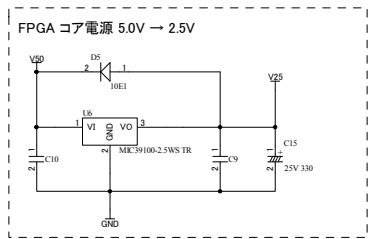
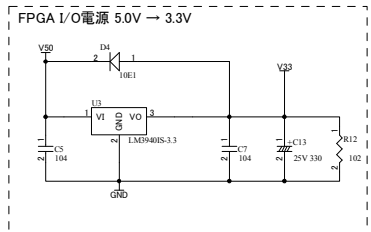
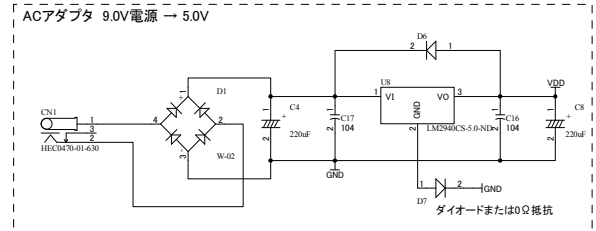
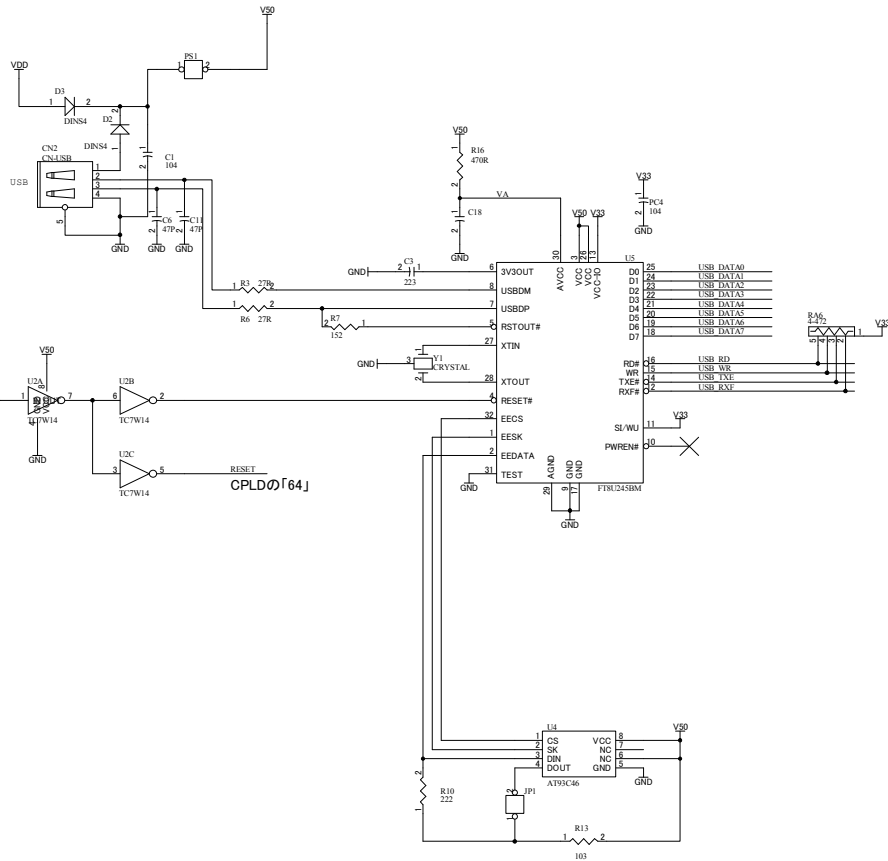
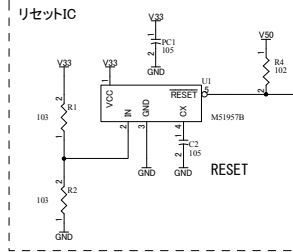
EDX001R2-SCH-E1.pdf

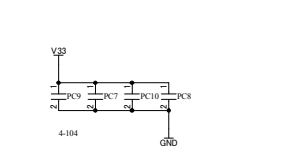
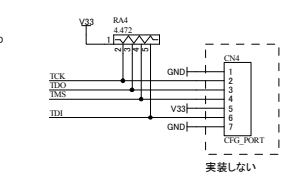
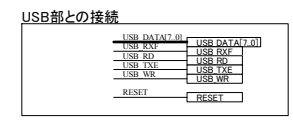
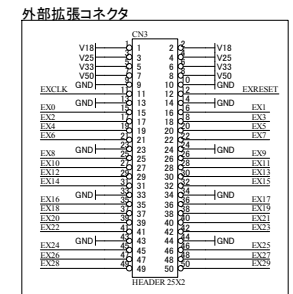
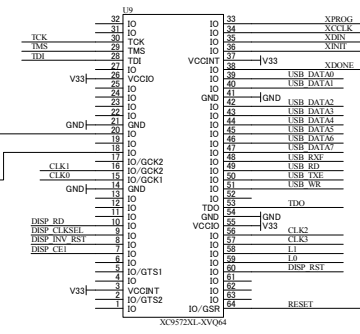
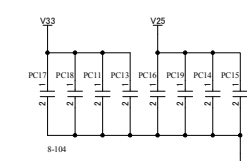
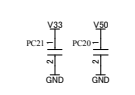
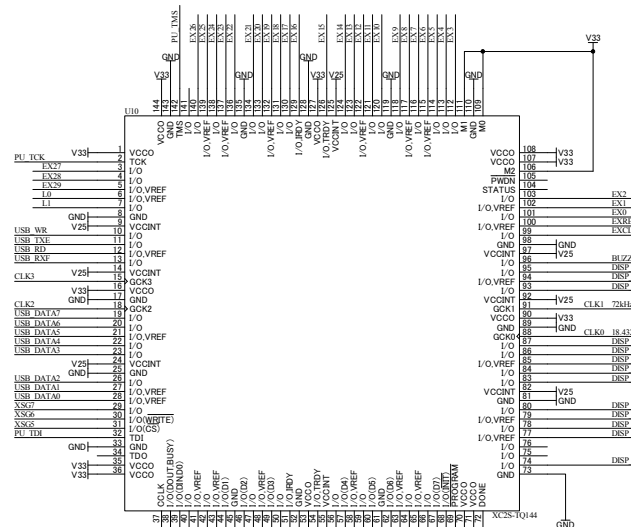
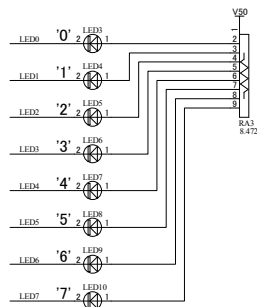
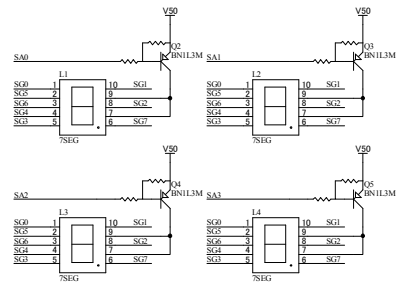
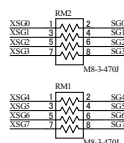
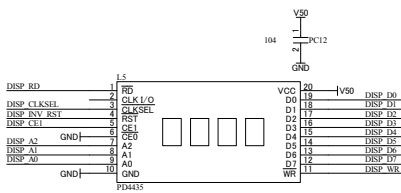
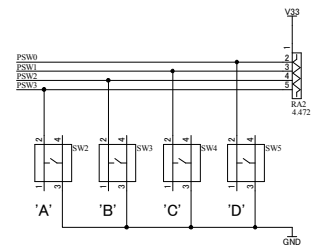
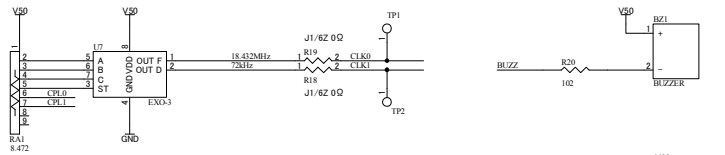
	-----		E1
	EDX-001 FPGA Trainer		
HuMANDATA LTD. OSAKA JAPAN www.hdl.co.jp/en/(Global) www.hdl.co.jp/(Japan)	DOC. No.	1	
Date: 30-Mar-2012	10:33:21	File: EDX_TOP.sch	Sheet 1 of 3


FPGA部との接続

USB_DATA7_01	USB_DATA[7_01]
USB_RN0	USB_RX0P
USB_RD0	USB_RX0N
USB_TN0	USB_TX0E
USB_WR	USB_WRN
RESET	RESET

リセットIC







HuMANDATA LTD.
OSAKA JAPAN
www.hdl.co.jp/en/(Global)
www.hdl.co.jp/(Japan)

EDX-001 FPGA Trainer

EDX001R2-SCH-E1.pdf

Date:	30-Mar-2012	10:33:21	File:	EDX_FPGA.Sch	
DOC. No.	3		Sheet	3 of 3	
			E1		