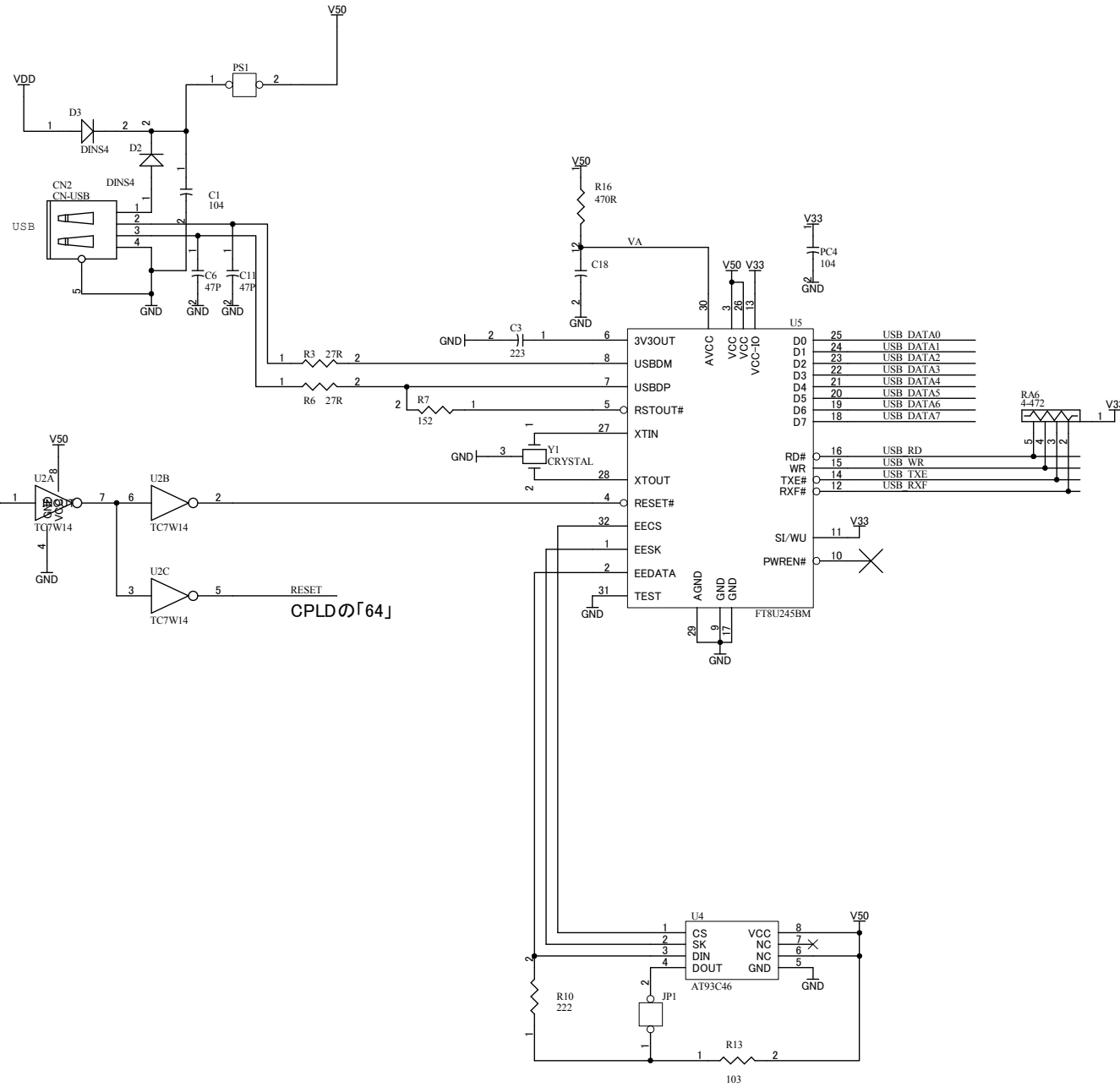
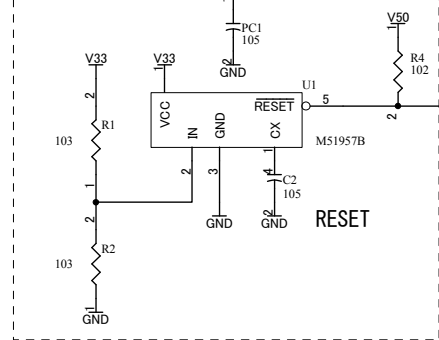
	2007/01/15		
		-----	
HuMANDATA LTD. OSAKA JAPAN www.hdl.co.jp		EDX-001 FPGA Trainer	
		DOC. No.	1
Date: 15-Jan-2007 16:08:48	File: EDX_TOP.sch	Sheet 1 of 3	E

FPGA部との接続

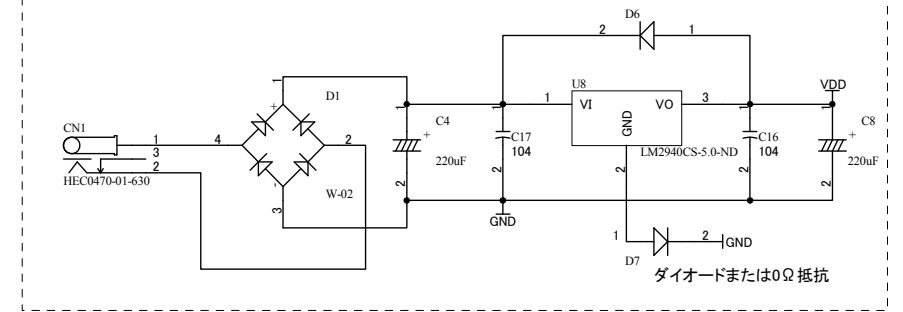
USB_DATA[7..0]	USB_DATA[7..0]
USB_RXF	USB_RXF
USB_RD	USB_RD
USB_TXE	USB_TXE
USB_WR	USB_WR
RESET	RESET



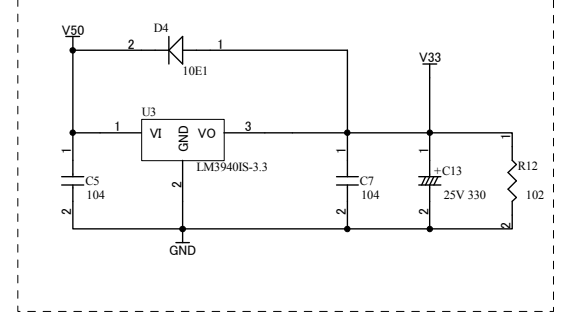
リセットIC



ACアダプタ 9.0V電源 → 5.0V



FPGA I/O電源 5.0V → 3.3V



FPGA コア電源 5.0V → 2.5V

