

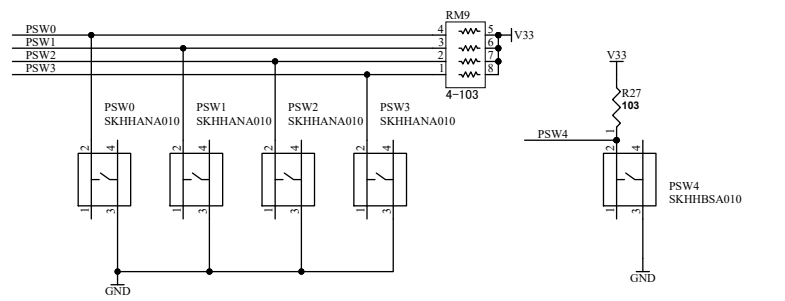
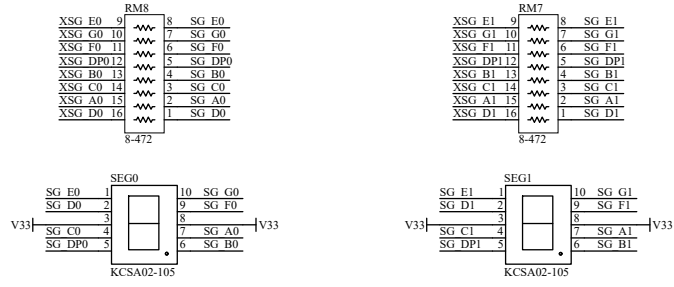
U FPGA FPGA.SchDoc	
ADBUS[0..7]	ADBUS[0..7]
ACBUS[0..7]	ACBUS[0..7]
CLK12L	CLK12L
CLK12R	CLK12R
X_DONE	X_DONE
XDCLK	XDCLK
XNCONFIG	XNCONFIG
XDATA	XDATA
XUSBRESET	XUSBRESET

EDA012R1-SCH-B3.pdf

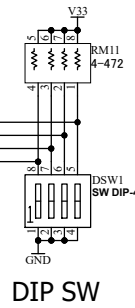


DSN:	TITLE: INTEL Cyclone 10 LP FPGA TRAINER
DOC No:	EDA-012
FILE: EDA012B.SchDoc	DATE: 2023/05/29 9:59:52
Sheet	B3 / 2

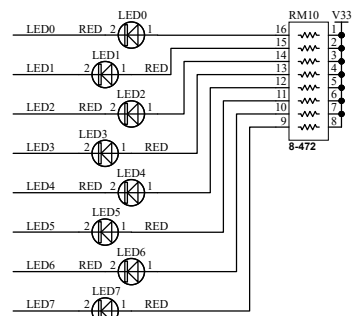
ADBUS[0..7]	ADBUS0..7
ACBUS[0..7]	ACBUS0..7
CLK12L	CLK12R
CLK12R	CLK12L
X_DONE	X_DONE
X_DONE	XDCLK
XDCLK	XNCONFIG
XNCONFIG	XDATA
XDATA	XUSBRESET
XUSBRESET	XUSBRESET



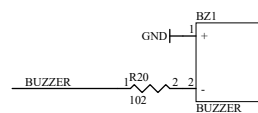
Push Switch



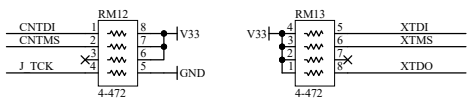
DIP SW



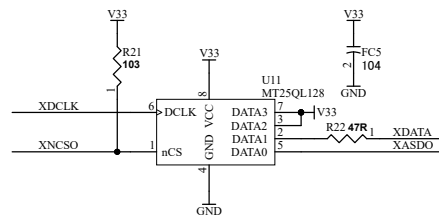
LED



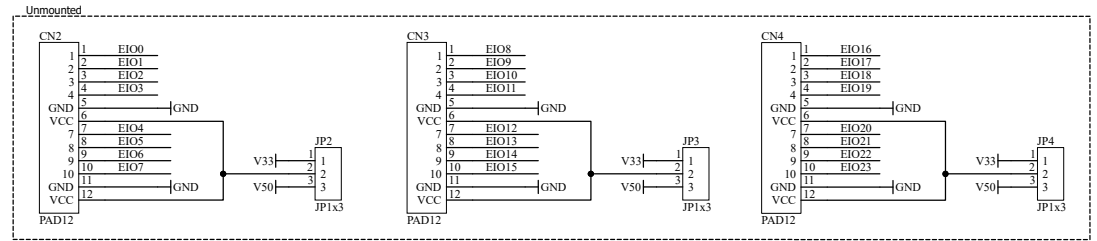
BUZZER



JTAG



Configuration ROM



ZKB-156

