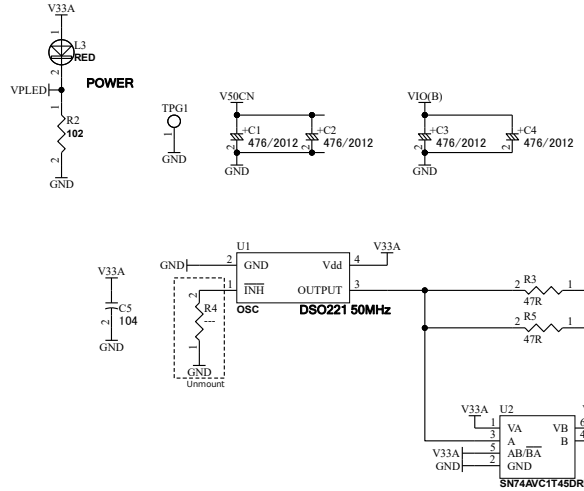
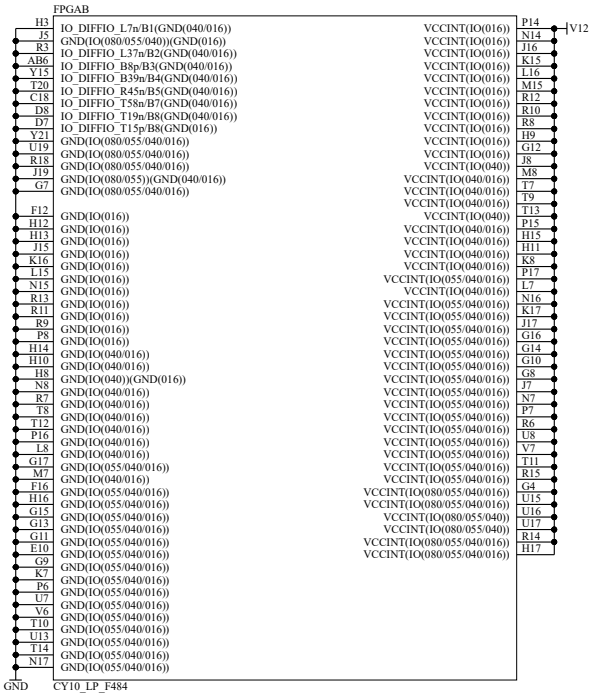
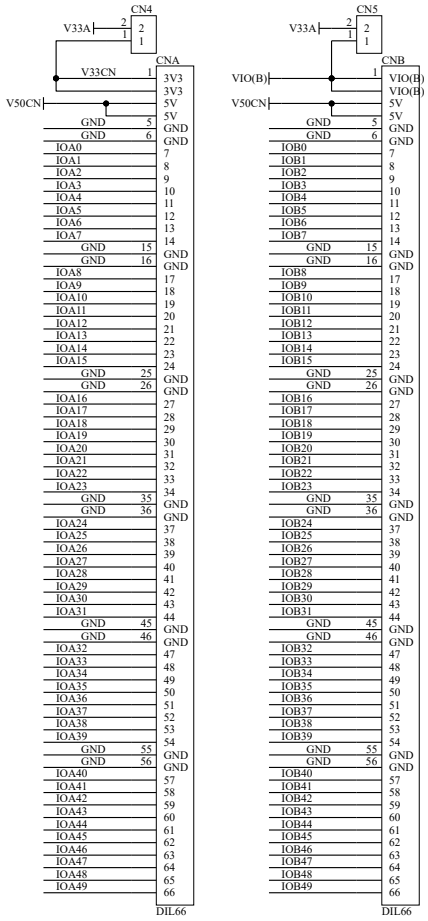
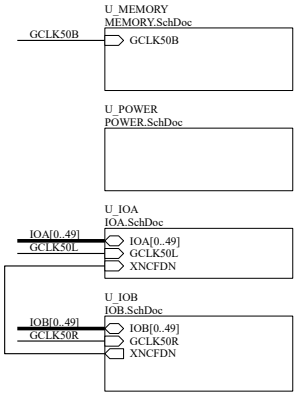






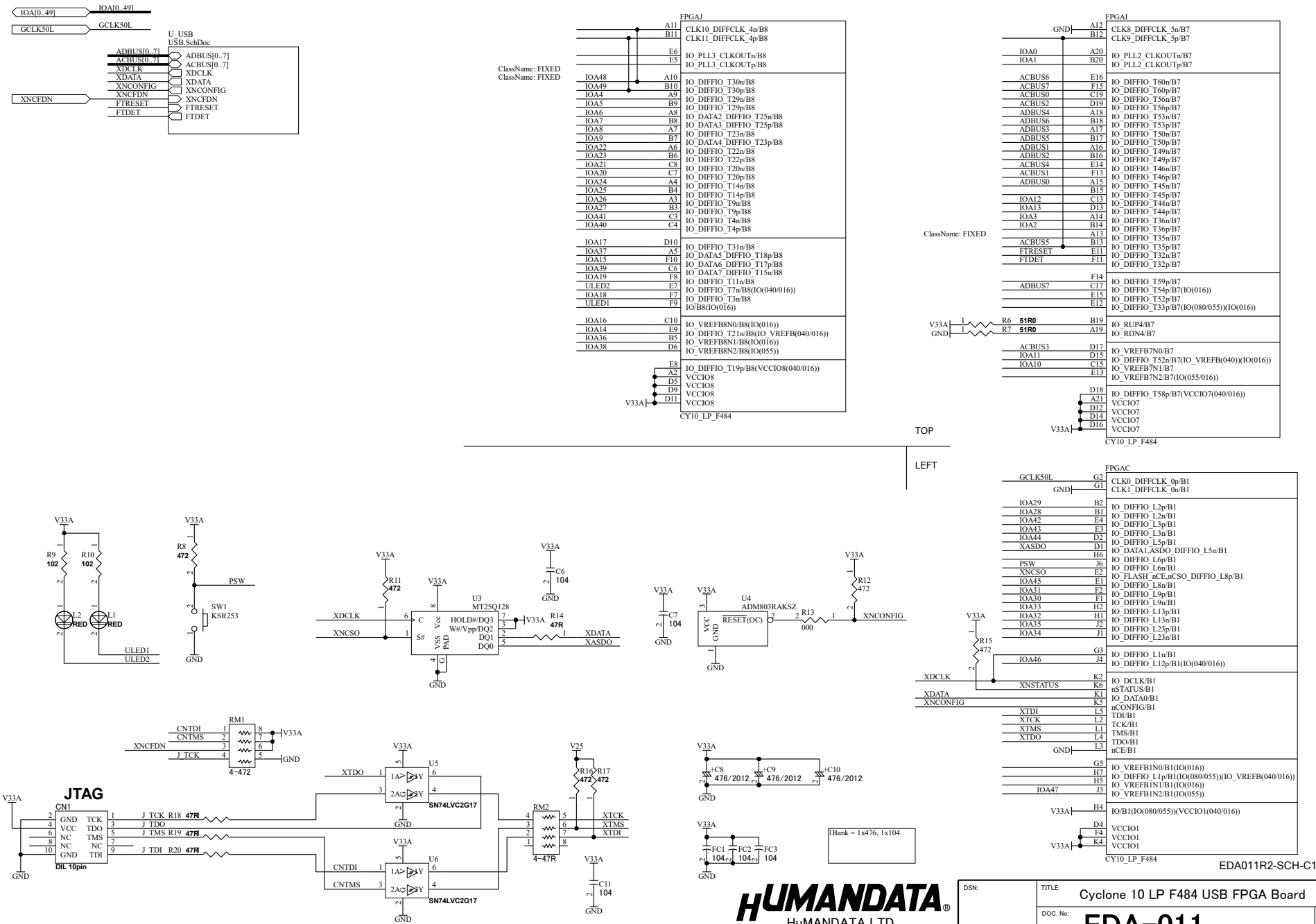


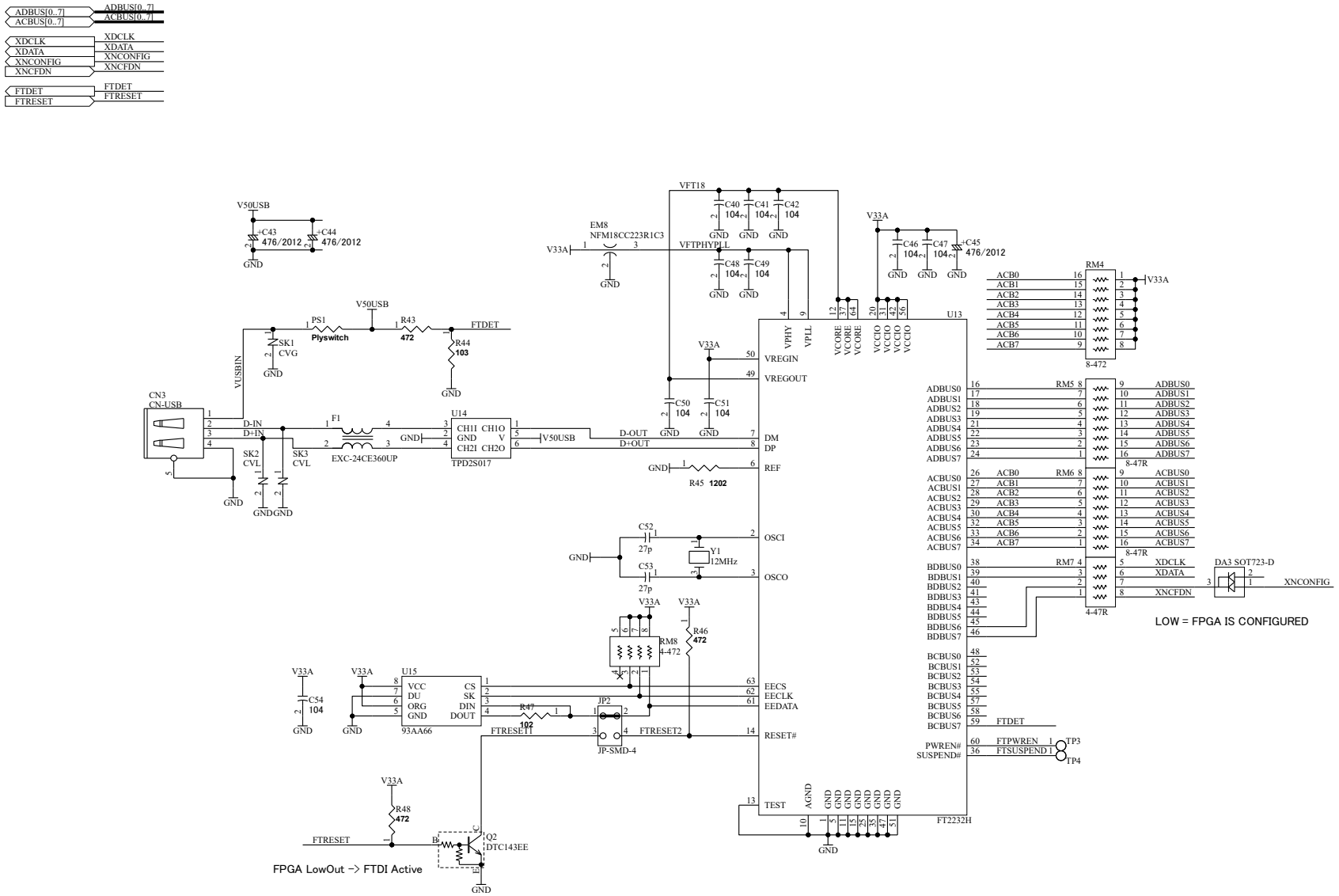
EDA011R2-SCH-C1.pdf

HuMANDATA LTD.
www.hdl.co.jp/ (Japan)
www2.hdl.co.jp/en/ (Global)

DSN:	TITLE: Cyclone 10 LP F484 USB FPGA Board	
	DOC. No: EDA-011	C1
	FILE: EDA011C.SchDoc DATE: 2026/09/07 10:49:06	Sheet: 1 / 6

V7_20200731


IOA[0..49]
GCLK50L
U_USB
USB.SchDoc
ADBUS[0..7]
ACBUS[0..7]
XDCLK
XDATA
XNCONFIG
XNCFDN
FTRESET
FTDET
XNCFDN
FPGAJ
ClassName: FIXED
ClassName: FIXED
CY10_LP_F484
FPGAI
ClassName: FIXED
CY10_LP_F484
TOP
LEFT
FPGAC
CY10_LP_F484
V33A
R9 102
R10 102
L2 RED
L1 RED
ULED1
ULED2
R8 472
PSW
SW1 KSR253
GND
R11 472
U3 MT25Q128
XDCLK
XNCSO
HOLD#/DQ3
W#/Vpp/DQ2
DQ1
DQ0
R14 47R
XDATA
XASDO
C6 104
C7 104
U4 ADM803RAKSZ
RESET(OC)
R13 000
R12 472
XNCONFIG
R15 472
RM1
CNTDI
CNTMS
XNCFDN
J_TCK
4-472
JTAG
CN1
GND TCK
VCC TDO
NC TMS
NC NC
GND TDI
J_TCK R18 47R
J_TDO
J_TMS R19 47R
J_TDI R20 47R
DIL 10pin
U5
U6
SN74LVC2G17
RM2
4-47R
R16 472
R17 472
XTCK
XTMS
XTDI
C11 104
C8 476/2012
C9 476/2012
C10 476/2012
FC1 104
FC2 104
FC3 104
1Bank = 1x476, 1x104
HUMANDATA
HuMANDATA LTD.
www.hdl.co.jp/ (Japan)
www2.hdl.co.jp/en/ (Global)
EDA011R2-SCH-C1.pdf
DSN:
TITLE: Cyclone 10 LP F484 USB FPGA Board
DOC. No: EDA-011
C1
FILE: IOA.SchDoc
DATE: 2026/09/07 10:49:06
Sheet: 2 / 6
V7_20200731

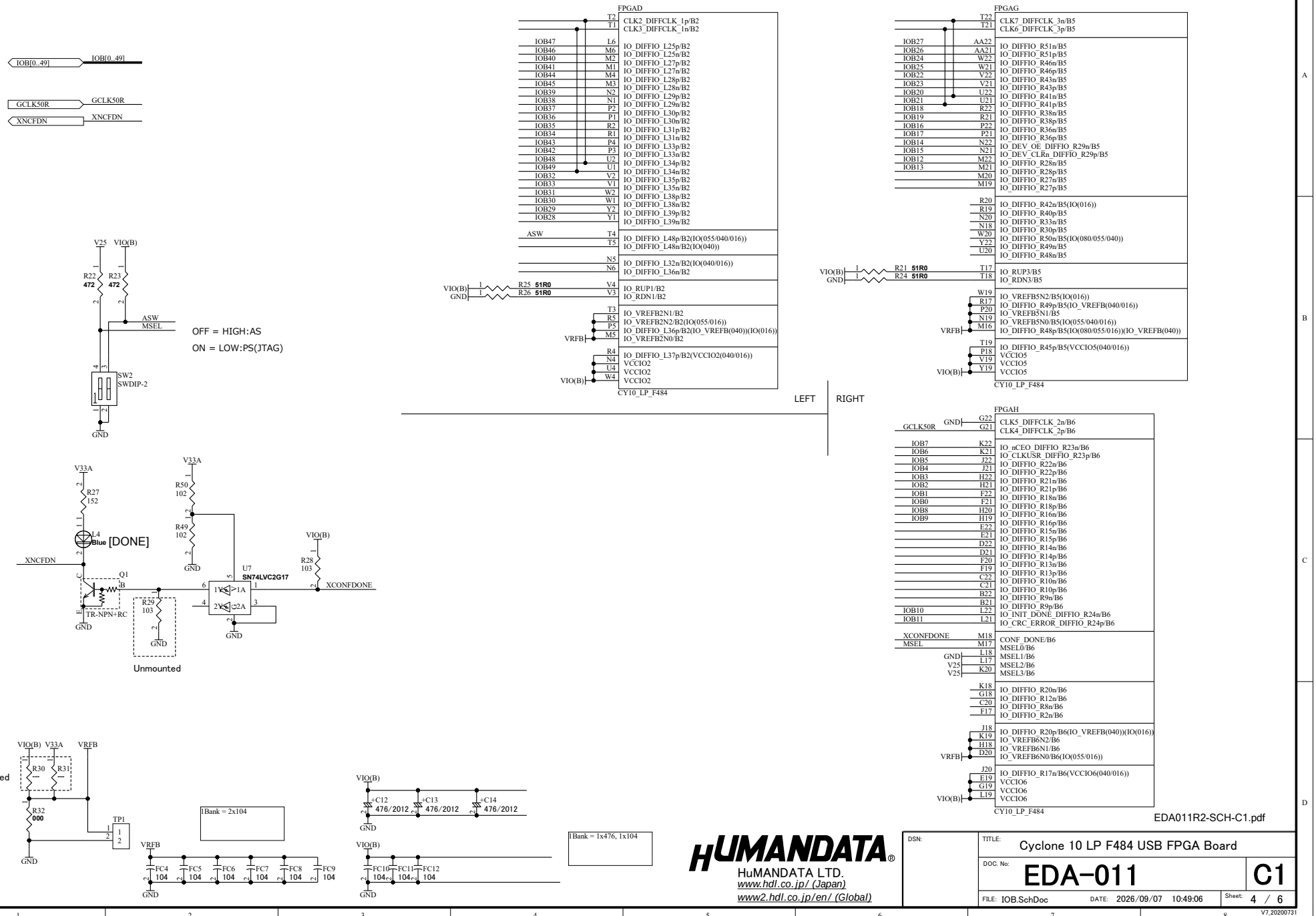


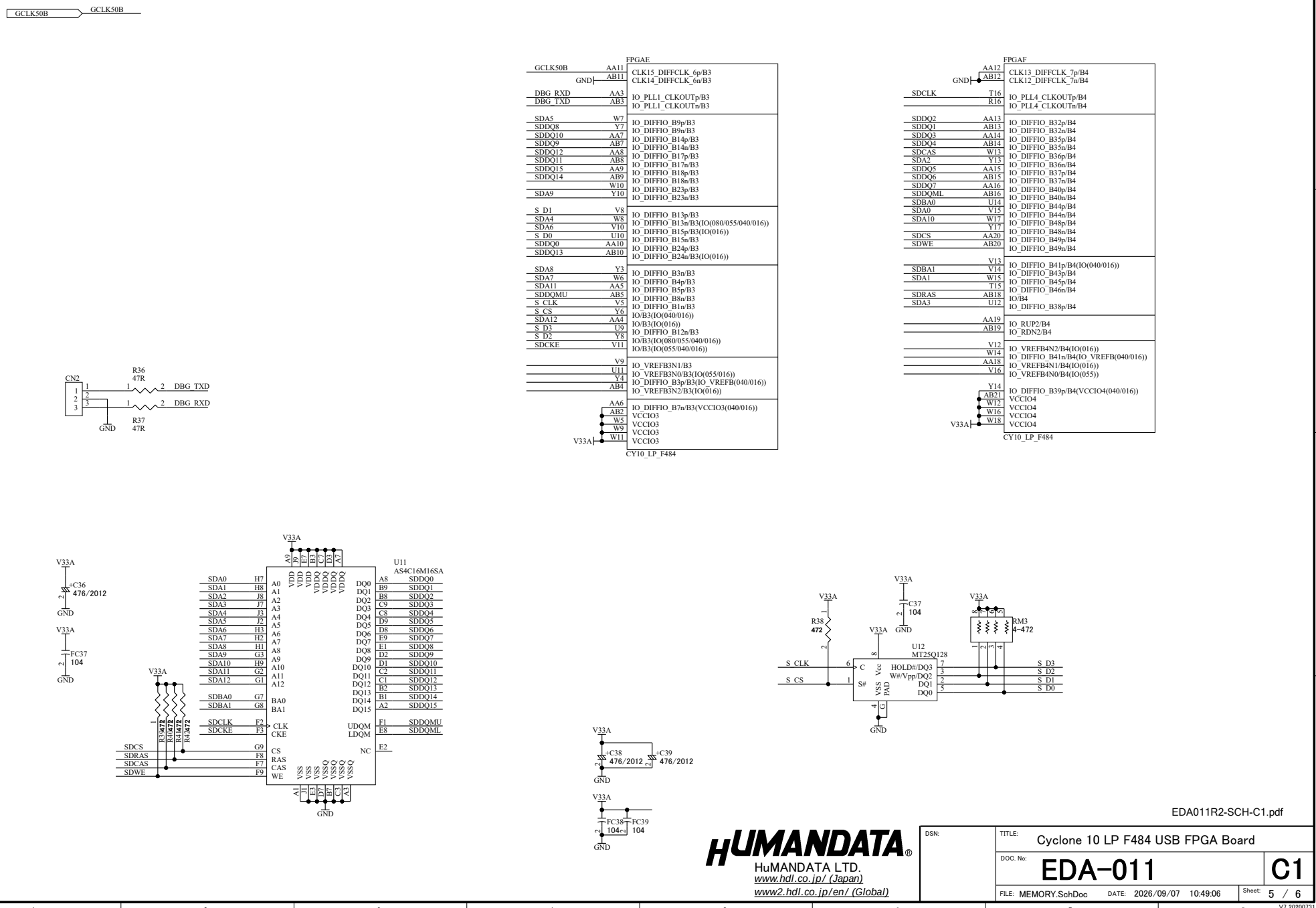
EDA011R2-SCH-C1.pdf

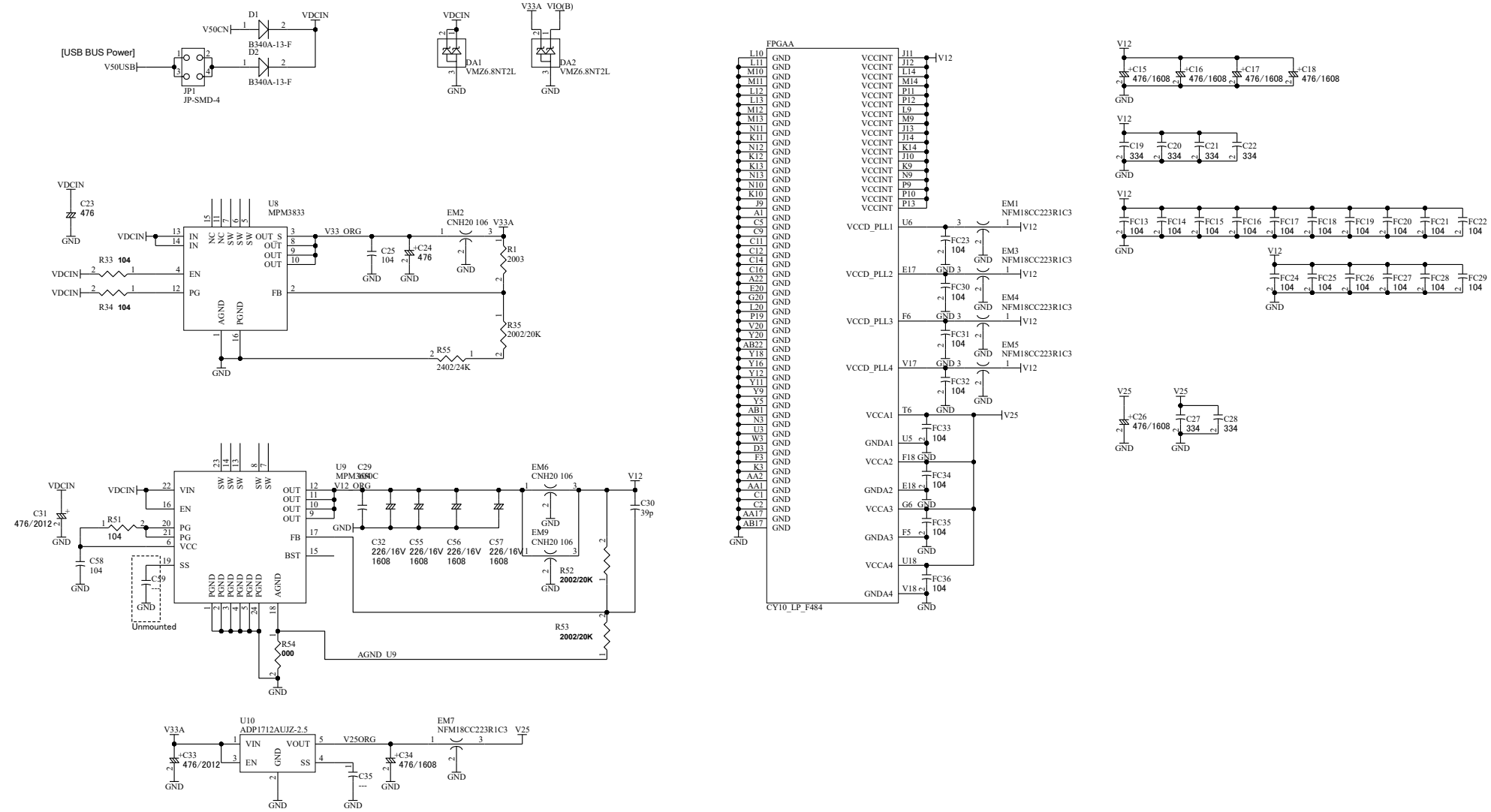
HuMANDATA LTD.
www.hdl.co.jp/ (Japan)
www2.hdl.co.jp/en/ (Global)

DSN:	TITLE: Cyclone 10 LP F484 USB FPGA Board	
	DOC. No: EDA-011	C1
	FILE: USB.SchDoc DATE: 2026/09/07 10:49:06	Sheet: 3 / 6

V7_20200731


IOB[0..49]
GCLK50R
XNCFDN
FPGAD
CLK2_DIFFCLK_1p/B2
CLK3_DIFFCLK_1n/B2
IO_DIFFIO_L25p/B2
IO_DIFFIO_L25n/B2
IO_DIFFIO_L27p/B2
IO_DIFFIO_L27n/B2
IO_DIFFIO_L28p/B2
IO_DIFFIO_L28n/B2
IO_DIFFIO_L29p/B2
IO_DIFFIO_L29n/B2
IO_DIFFIO_L30p/B2
IO_DIFFIO_L30n/B2
IO_DIFFIO_L31p/B2
IO_DIFFIO_L31n/B2
IO_DIFFIO_L33p/B2
IO_DIFFIO_L33n/B2
IO_DIFFIO_L34p/B2
IO_DIFFIO_L34n/B2
IO_DIFFIO_L35p/B2
IO_DIFFIO_L35n/B2
IO_DIFFIO_L38p/B2
IO_DIFFIO_L38n/B2
IO_DIFFIO_L39p/B2
IO_DIFFIO_L39n/B2
IO_DIFFIO_L48p/B2(IO(055/040/016))
IO_DIFFIO_L48n/B2(IO(040))
IO_DIFFIO_L32n/B2(IO(040/016))
IO_DIFFIO_L36n/B2
IO_RUP1/B2
IO_RDN1/B2
IO_VREFB2N1/B2
IO_VREFB2N2/B2(IO(055/016))
IO_DIFFIO_L36p/B2(IO_VREFB(040))(IO(016))
IO_VREFB2N0/B2
IO_DIFFIO_L37p/B2(VCCIO2(040/016))
VCCIO2
CY10_LP_F484
FPGAG
CLK7_DIFFCLK_3n/B5
CLK6_DIFFCLK_3p/B5
IO_DIFFIO_R51n/B5
IO_DIFFIO_R51p/B5
IO_DIFFIO_R46n/B5
IO_DIFFIO_R46p/B5
IO_DIFFIO_R43n/B5
IO_DIFFIO_R43p/B5
IO_DIFFIO_R41n/B5
IO_DIFFIO_R41p/B5
IO_DIFFIO_R38n/B5
IO_DIFFIO_R38p/B5
IO_DIFFIO_R36n/B5
IO_DIFFIO_R36p/B5
IO_DEV_OE_DIFFIO_R29n/B5
IO_DEV_CLRn_DIFFIO_R29p/B5
IO_DIFFIO_R28n/B5
IO_DIFFIO_R28p/B5
IO_DIFFIO_R27n/B5
IO_DIFFIO_R27p/B5
IO_DIFFIO_R42n/B5(IO(016))
IO_DIFFIO_R40p/B5
IO_DIFFIO_R33n/B5
IO_DIFFIO_R30p/B5
IO_DIFFIO_R50n/B5(IO(080/055/040))
IO_DIFFIO_R49n/B5
IO_DIFFIO_R48n/B5
R21 51R0
R24 51R0
IO_RUP3/B5
IO_RDN3/B5
IO_VREFB5N2/B5(IO(016))
IO_DIFFIO_R49p/B5(IO_VREFB(040/016))
IO_VREFB5N1/B5
IO_VREFB5N0/B5(IO(055/040/016))
IO_DIFFIO_R48p/B5(IO(080/055/016))(IO_VREFB(040))
IO_DIFFIO_R45p/B5(VCCIO5(040/016))
VCCIO5
CY10_LP_F484
LEFT
RIGHT
FPGAH
CLK5_DIFFCLK_2n/B6
CLK4_DIFFCLK_2p/B6
IO_nCEO_DIFFIO_R23n/B6
IO_CLKUSR_DIFFIO_R23p/B6
IO_DIFFIO_R22n/B6
IO_DIFFIO_R22p/B6
IO_DIFFIO_R21n/B6
IO_DIFFIO_R21p/B6
IO_DIFFIO_R18n/B6
IO_DIFFIO_R18p/B6
IO_DIFFIO_R16n/B6
IO_DIFFIO_R16p/B6
IO_DIFFIO_R15n/B6
IO_DIFFIO_R15p/B6
IO_DIFFIO_R14n/B6
IO_DIFFIO_R14p/B6
IO_DIFFIO_R13n/B6
IO_DIFFIO_R13p/B6
IO_DIFFIO_R10n/B6
IO_DIFFIO_R10p/B6
IO_DIFFIO_R9n/B6
IO_DIFFIO_R9p/B6
IO_INIT_DONE_DIFFIO_R24n/B6
IO_CRC_ERROR_DIFFIO_R24p/B6
CONF_DONE/B6
MSEL0/B6
MSEL1/B6
MSEL2/B6
MSEL3/B6
IO_DIFFIO_R20n/B6
IO_DIFFIO_R12n/B6
IO_DIFFIO_R8n/B6
IO_DIFFIO_R2n/B6
IO_DIFFIO_R20p/B6(IO_VREFB(040))(IO(016))
IO_VREFB6N2/B6
IO_VREFB6N1/B6
IO_VREFB6N0/B6(IO(055/016))
IO_DIFFIO_R17n/B6(VCCIO6(040/016))
VCCIO6
CY10_LP_F484
EDA011R2-SCH-C1.pdf
R22 472
R23 472
ASW
MSEL
SW2
SWDIP-2
OFF = HIGH:AS
ON = LOW:PS(JTAG)
R27 152
L4 Blue [DONE]
Q1
TR-NPN+RC
R50 102
R49 102
U7 SN74LVC2G17
R28 103
XCONFDONE
R29 103
Unmounted
R30 ---
R31 ---
R32 000
TP1
1Bank = 2x104
FC4 104
FC5 104
FC6 104
FC7 104
FC8 104
FC9 104
+C12 476/2012
+C13 476/2012
+C14 476/2012
FC10 104
FC11 104
FC12 104
1Bank = 1x476, 1x104
HUMANDATA
HuMANDATA LTD.
www.hdl.co.jp/ (Japan)
www2.hdl.co.jp/en/ (Global)
DSN:
TITLE: Cyclone 10 LP F484 USB FPGA Board
DOC. No: EDA-011
C1
FILE: IOB.SchDoc
DATE: 2026/09/07 10:49:06
Sheet: 4 / 6
V7_20200731


GCLK50B
GCLK50B
FPGAE
GCLK50B AA11 CLK15_DIFFCLK_6p/B3
GND AB11 CLK14_DIFFCLK_6n/B3
DBG_RXD AA3 IO_PLL1_CLKOUTp/B3
DBG_TXD AB3 IO_PLL1_CLKOUTn/B3
SDA5 W7 IO_DIFFIO_B9p/B3
SDDQ8 Y7 IO_DIFFIO_B9n/B3
SDDQ10 AA7 IO_DIFFIO_B14p/B3
SDDQ9 AB7 IO_DIFFIO_B14n/B3
SDDQ12 AA8 IO_DIFFIO_B17p/B3
SDDQ11 AB8 IO_DIFFIO_B17n/B3
SDDQ15 AA9 IO_DIFFIO_B18p/B3
SDDQ14 AB9 IO_DIFFIO_B18n/B3
W10 IO_DIFFIO_B23p/B3
SDA9 Y10 IO_DIFFIO_B23n/B3
S_D1 V8 IO_DIFFIO_B13p/B3
SDA4 W8 IO_DIFFIO_B13n/B3(IO(080/055/040/016))
SDA6 V10 IO_DIFFIO_B15p/B3(IO(016))
S_D0 U10 IO_DIFFIO_B15n/B3
SDDQ0 AA10 IO_DIFFIO_B24p/B3
SDDQ13 AB10 IO_DIFFIO_B24n/B3(IO(016))
SDA8 Y3 IO_DIFFIO_B3n/B3
SDA7 W6 IO_DIFFIO_B4p/B3
SDA11 AA5 IO_DIFFIO_B5p/B3
SDDQMU AB5 IO_DIFFIO_B8n/B3
S_CLK V5 IO_DIFFIO_B1n/B3
S_CS Y6 IO/B3(IO(040/016))
SDA12 AA4 IO/B3(IO(016))
S_D3 U9 IO_DIFFIO_B12n/B3
S_D2 Y8 IO/B3(IO(080/055/040/016))
SDCKE V11 IO/B3(IO(055/040/016))
V9 IO_VREFB3N1/B3
U11 IO_VREFB3N0/B3(IO(055/016))
Y4 IO_DIFFIO_B3p/B3(IO_VREFB(040/016))
AB4 IO_VREFB3N2/B3(IO(016))
AA6 IO_DIFFIO_B7n/B3(VCCIO3(040/016))
AB2 VCCIO3
W5 VCCIO3
W9 VCCIO3
V33A W11 VCCIO3
CY10_LP_F484
FPGAF
AA12 CLK13_DIFFCLK_7p/B4
GND AB12 CLK12_DIFFCLK_7n/B4
SDCLK T16 IO_PLL4_CLKOUTp/B4
R16 IO_PLL4_CLKOUTn/B4
SDDQ2 AA13 IO_DIFFIO_B32p/B4
SDDQ1 AB13 IO_DIFFIO_B32n/B4
SDDQ3 AA14 IO_DIFFIO_B35p/B4
SDDQ4 AB14 IO_DIFFIO_B35n/B4
SDCAS W13 IO_DIFFIO_B36p/B4
SDA2 Y13 IO_DIFFIO_B36n/B4
SDDQ5 AA15 IO_DIFFIO_B37p/B4
SDDQ6 AB15 IO_DIFFIO_B37n/B4
SDDQ7 AA16 IO_DIFFIO_B40p/B4
SDDQML AB16 IO_DIFFIO_B40n/B4
SDBA0 U14 IO_DIFFIO_B44p/B4
SDA0 V15 IO_DIFFIO_B44n/B4
SDA10 W17 IO_DIFFIO_B48p/B4
Y17 IO_DIFFIO_B48n/B4
SDCS AA20 IO_DIFFIO_B49p/B4
SDWE AB20 IO_DIFFIO_B49n/B4
V13 IO_DIFFIO_B41p/B4(IO(040/016))
SDBA1 V14 IO_DIFFIO_B43p/B4
SDA1 W15 IO_DIFFIO_B45p/B4
T15 IO_DIFFIO_B46n/B4
SDRAS AB18 IO/B4
SDA3 U12 IO_DIFFIO_B38p/B4
AA19 IO_RUP2/B4
AB19 IO_RDN2/B4
V12 IO_VREFB4N2/B4(IO(016))
W14 IO_DIFFIO_B41n/B4(IO_VREFB(040/016))
AA18 IO_VREFB4N1/B4(IO(016))
V16 IO_VREFB4N0/B4(IO(055))
Y14 IO_DIFFIO_B39p/B4(VCCIO4(040/016))
AB21 VCCIO4
W12 VCCIO4
W16 VCCIO4
V33A W18 VCCIO4
CY10_LP_F484
CN2
R36 47R
DBG_TXD
R37 47R
DBG_RXD
GND
V33A
C36 476/2012
FC37 104
GND
U11 AS4C16M16SA
SDA0 H7 A0 DQ0 A8 SDDQ0
SDA1 H8 A1 DQ1 B9 SDDQ1
SDA2 J8 A2 DQ2 B8 SDDQ2
SDA3 J7 A3 DQ3 C9 SDDQ3
SDA4 J3 A4 DQ4 C8 SDDQ4
SDA5 J2 A5 DQ5 D9 SDDQ5
SDA6 H3 A6 DQ6 D8 SDDQ6
SDA7 H2 A7 DQ7 E9 SDDQ7
SDA8 H1 A8 DQ8 E1 SDDQ8
SDA9 G3 A9 DQ9 D2 SDDQ9
SDA10 H9 A10 DQ10 D1 SDDQ10
SDA11 G2 A11 DQ11 C2 SDDQ11
SDA12 G1 A12 DQ12 C1 SDDQ12
DQ13 B2 SDDQ13
SDBA0 G7 BA0 DQ14 B1 SDDQ14
SDBA1 G8 BA1 DQ15 A2 SDDQ15
SDCLK F2 CLK UDQM F1 SDDQMU
SDCKE F3 CKE LDQM E8 SDDQML
NC E2
SDCS G9 CS
SDRAS F8 RAS
SDCAS F7 CAS
SDWE F9 WE
VDD VSS VDDQ VSSQ
R34 472 R35 472 R40 472 R43 472
V33A
GND
V33A
C38 476/2012
C39 476/2012
GND
V33A
FC38 104
FC39 104
GND
V33A
R38 472
C37 104
GND
V33A
RM3 4-472
U12 MT25Q128
S_CLK
S_CS
C
S#
Vcc
VSS
PAD
HOLD#/DQ3
W#/Vpp/DQ2
DQ1
DQ0
S_D3
S_D2
S_D1
S_D0
GND
EDA011R2-SCH-C1.pdf
HuMANDATA LTD.
www.hdl.co.jp/ (Japan)
www2.hdl.co.jp/en/ (Global)
DSN:
TITLE: Cyclone 10 LP F484 USB FPGA Board
DOC. No: EDA-011
C1
FILE: MEMORY.SchDoc
DATE: 2026/09/07 10:49:06
Sheet: 5 / 6
V7_20200731



EDA011R2-SCH-C1.pdf

HuMANDATA LTD.
www.hdl.co.jp/ (Japan)
www2.hdl.co.jp/en/ (Global)

DSN:	TITLE: Cyclone 10 LP F484 USB FPGA Board	
	DOC. No: EDA-011	C1
	FILE: POWER.SchDoc DATE: 2026/09/07 10:49:06	Sheet: 6 / 6

V7_20200731