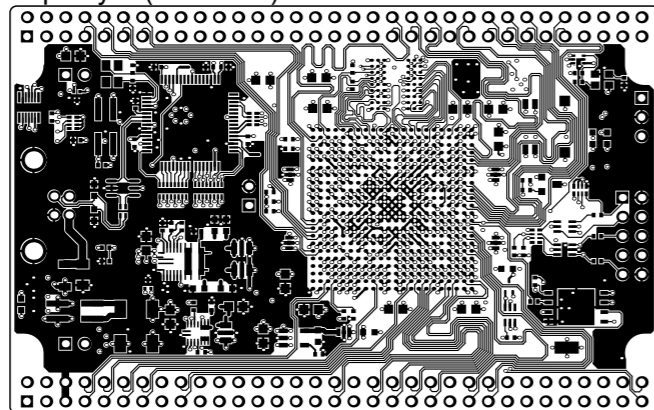


1 2 3 4 5 6 7 8

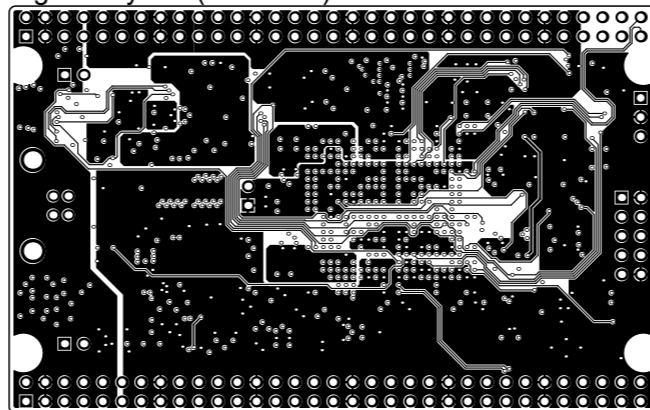
A

A

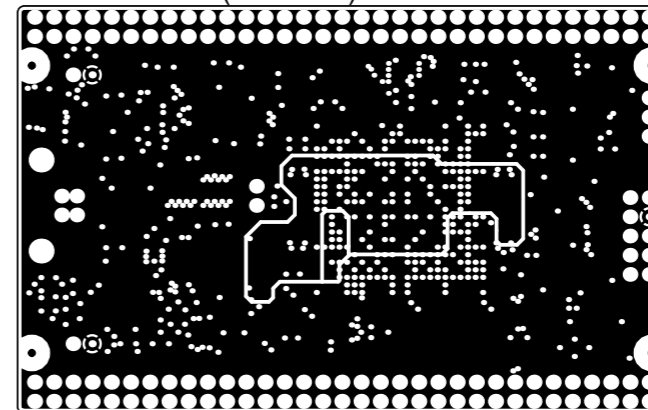
Top Layer (Scale 1:1)



Signal Layer 1 (Scale 1:1)



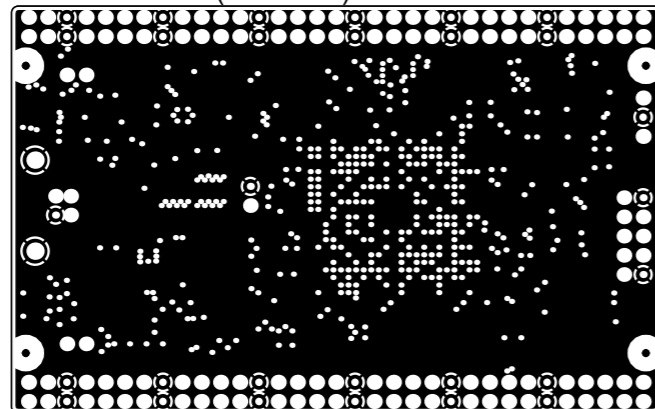
Internal Plane 2 (Scale 1:1)



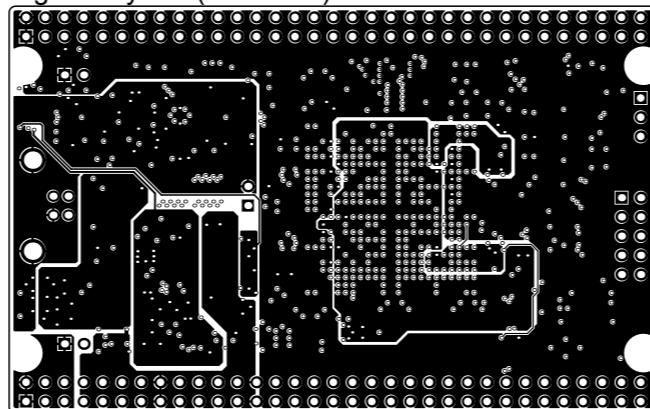
B

B

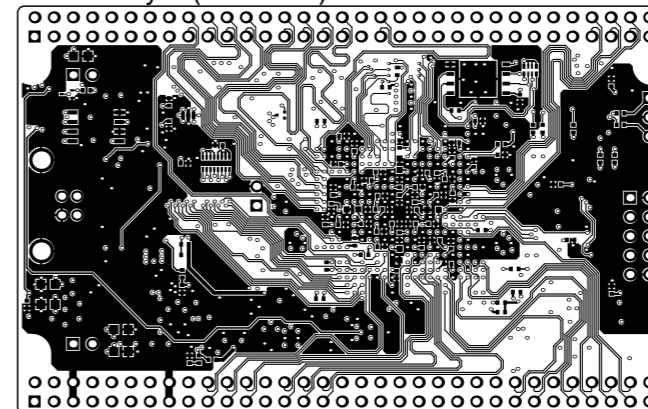
Internal Plane 1 (Scale 1:1)



Signal Layer 2 (Scale 1:1)



Bottom Layer (Scale 1:1)



C

C

PCB Version : C

D

D



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DSN

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EDA-011 PCB Drawing

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EDA011R2-PCB-C

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DATE: 2022/07/27

Sheet

2 / 2

1 2 3 4 5 6 7 8

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