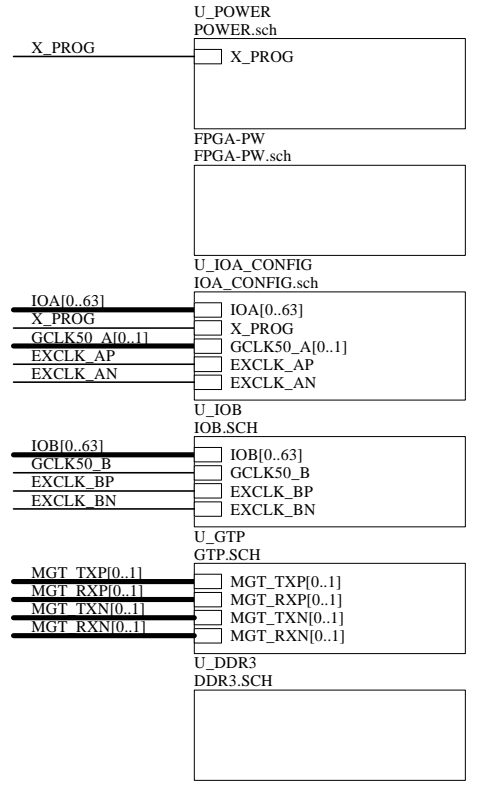
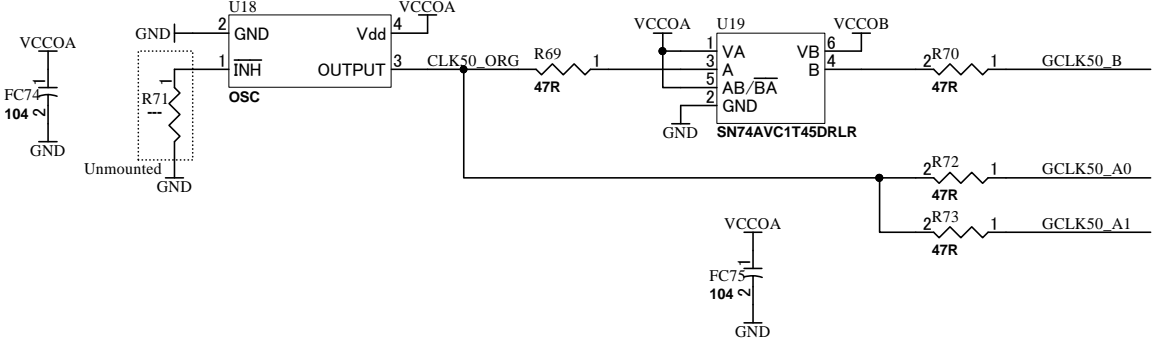
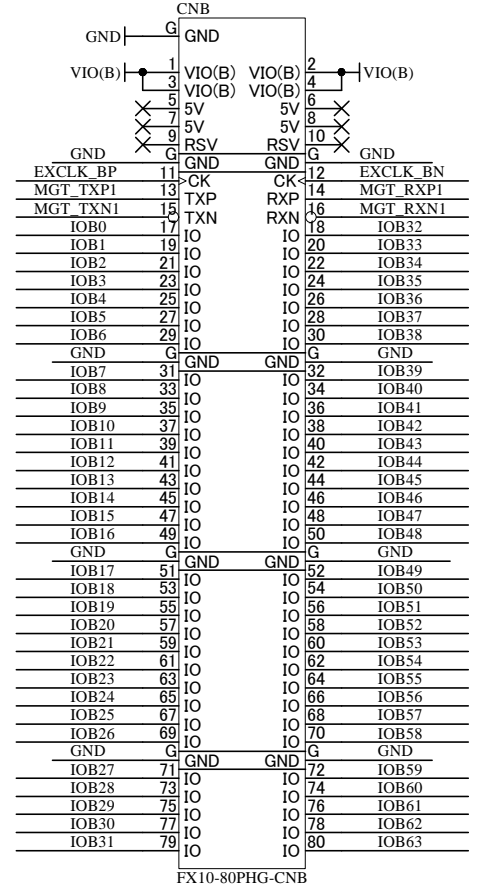
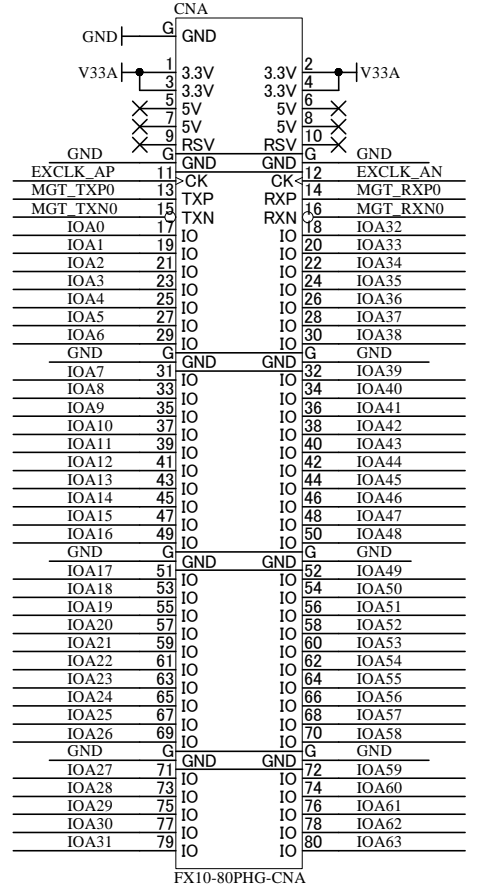
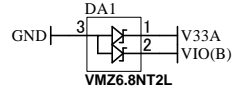
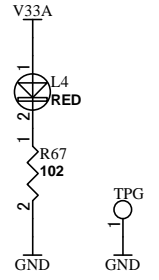


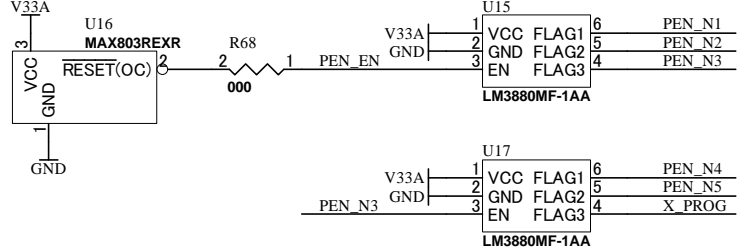
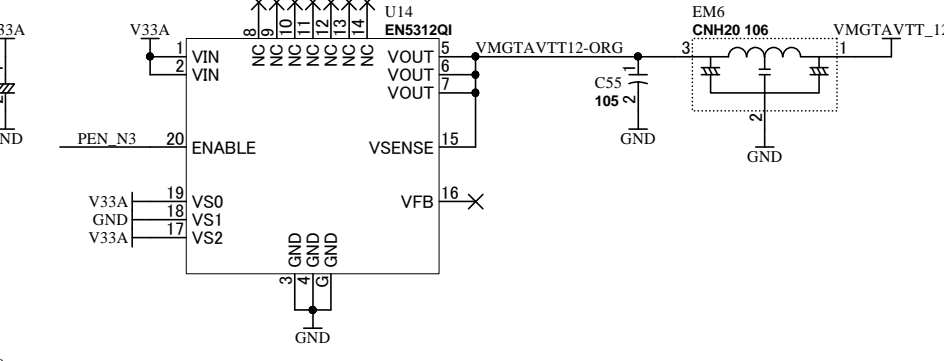
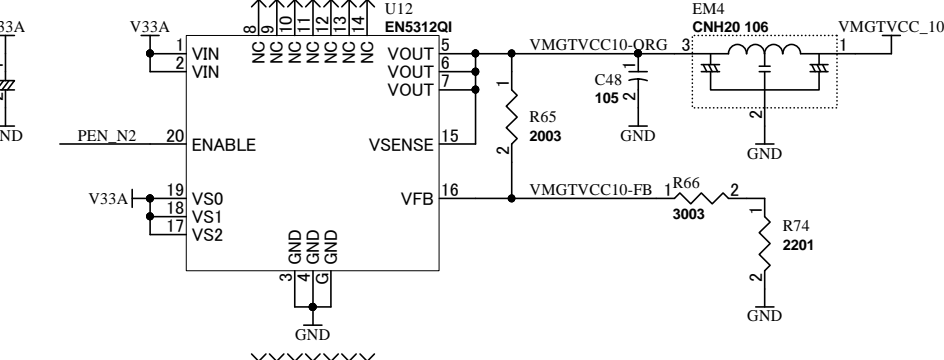
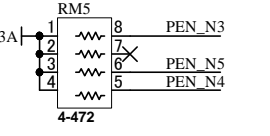
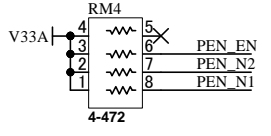
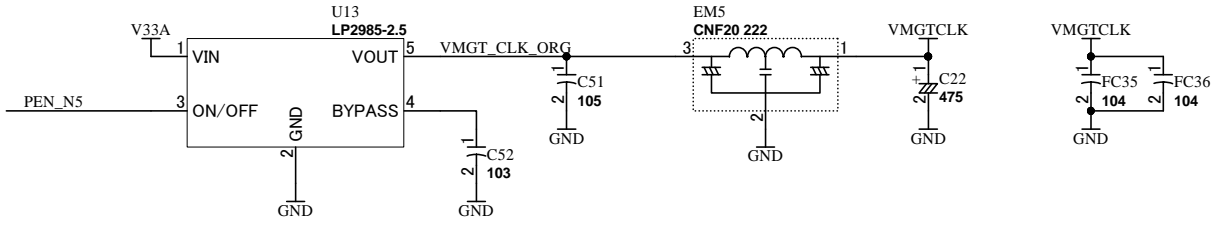
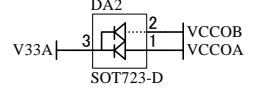
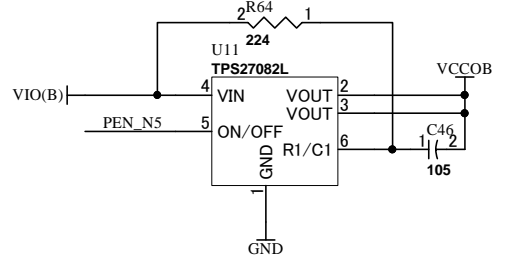
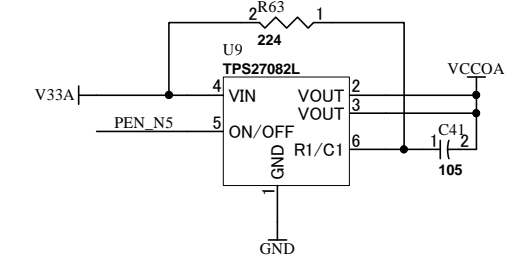
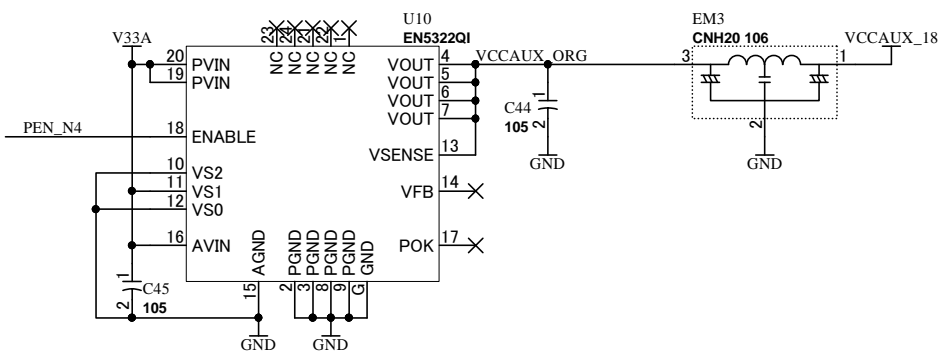
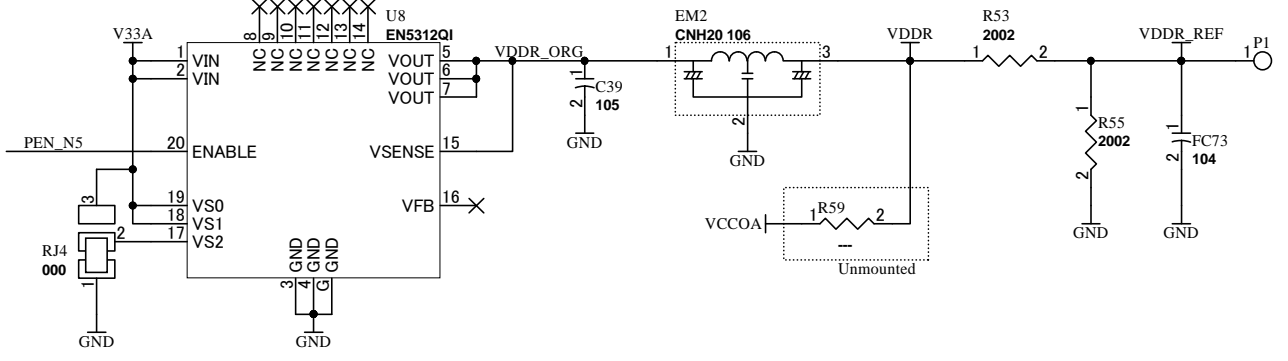
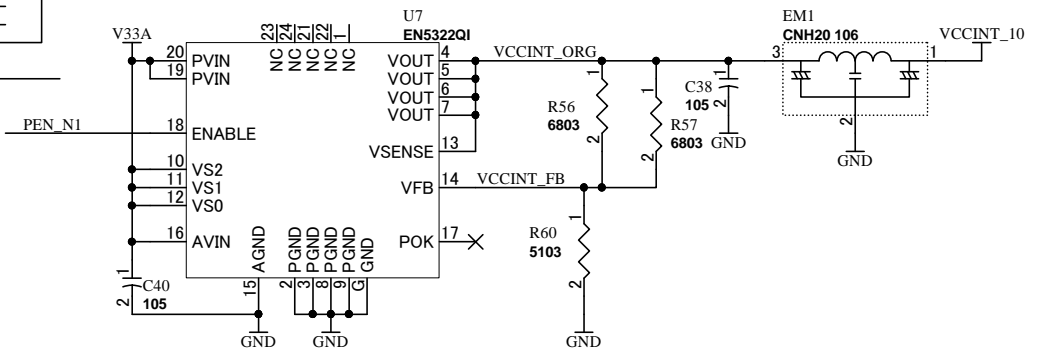
V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VCCAUX_18	VCCAUX_18
VMGTAVTT_12	VMGTAVTT_12
VMGTVCC_10	VMGTVCC_10
VMGTCLK	VMGTCLK
VDDR	VDDR
VCCOB	VCCOB
VCCOA	VCCOA
GND	GND

[POWER]



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		Sheet 1 of 7

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VCCAUX_18	VCCAUX_18
VMGTAVTT_12	VMGTAVTT_12
VMGTVCC_10	VMGTVCC_10
VMGTCLK	VMGTCLK
VDDR	VDDR
VCCOB	VCCOB
VCCOA	VCCOA
GND	GND



Power sense point

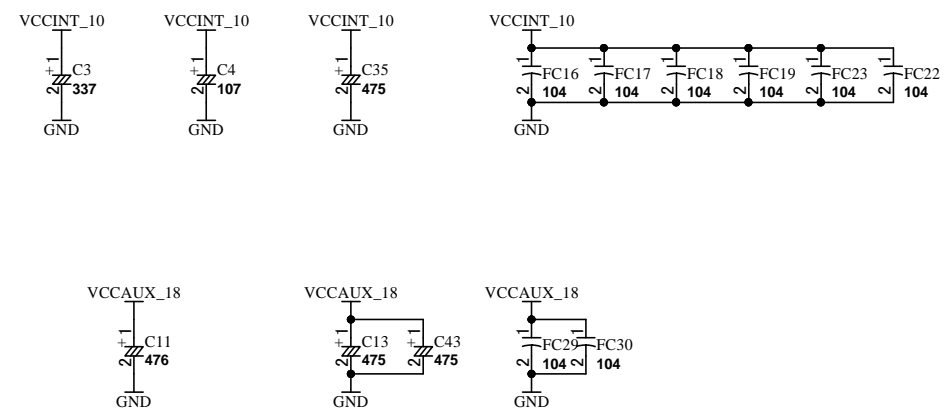
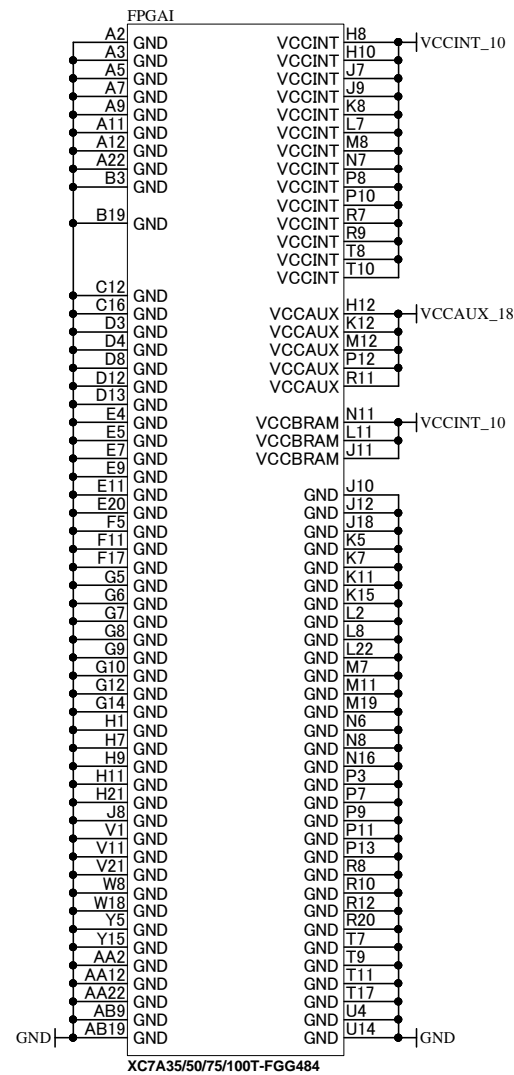
1	GND
2	VCCINT_10
3	VCCAUX_18
4	VMGTAVTT_12
5	VMGTVCC_10
6	VMGTCLK
7	VCCOB
8	VDDR
9	VCCOA
10	GND

TP2

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V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VCCAUX_18	VCCAUX_18
VMGTAVTT_12	VMGTAVTT_12
VMGTAVCC_10	VMGTAVCC_10
VMGTCLK	VMGTCLK
VDDR	VDDR
VCCOB	VCCOB
VCCOA	VCCOA
GND	GND



	ARTIX-7 FBG484 FPGA Board	
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V33A	VIO(B)	VCCINT_10	VCCINT_18	VMGTAVTT_12	VMGTAVTT_10	VMGTVCC_10	VMGTCLK	VDDR	VCCOB	VCCOA	GND
V33A	VIO(B)	VCCINT_10	VCCINT_18	VMGTAVTT_12	VMGTAVTT_10	VMGTVCC_10	VMGTCLK	VDDR	VCCOB	VCCOA	GND

IOA[0..63]	IOA0..63
GCLK50 A[0..1]	GCLK50 A0..11
X_PROG	X_PROG
EXCLK_AP	EXCLK_AP
EXCLK_AN	EXCLK_AN

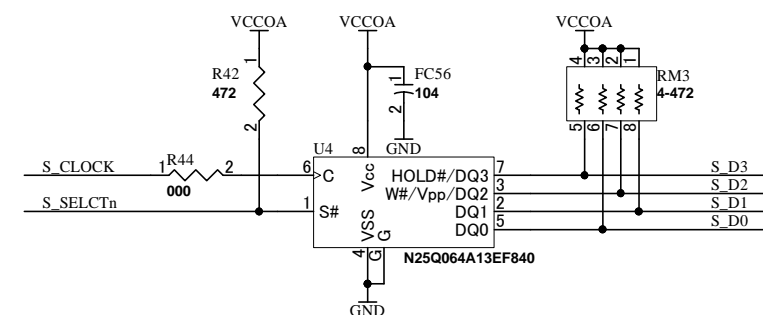
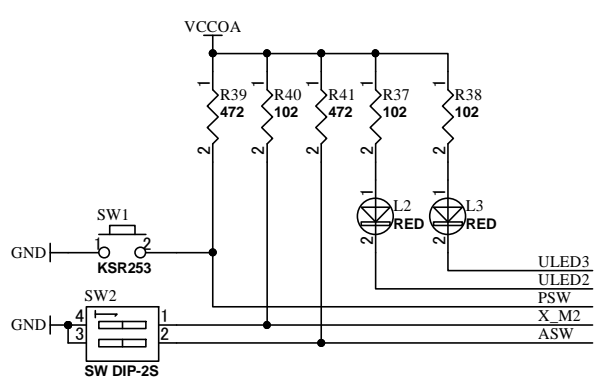
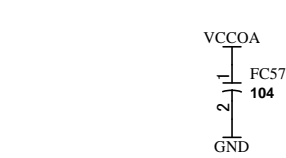
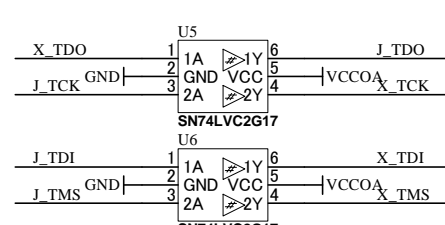
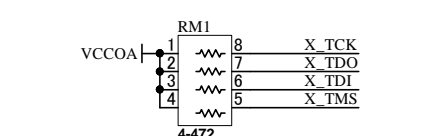
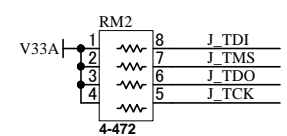
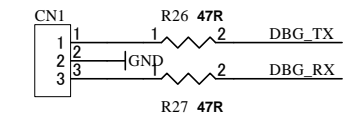
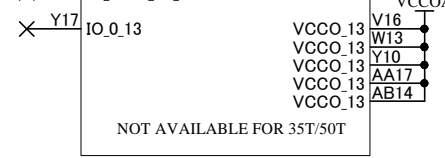
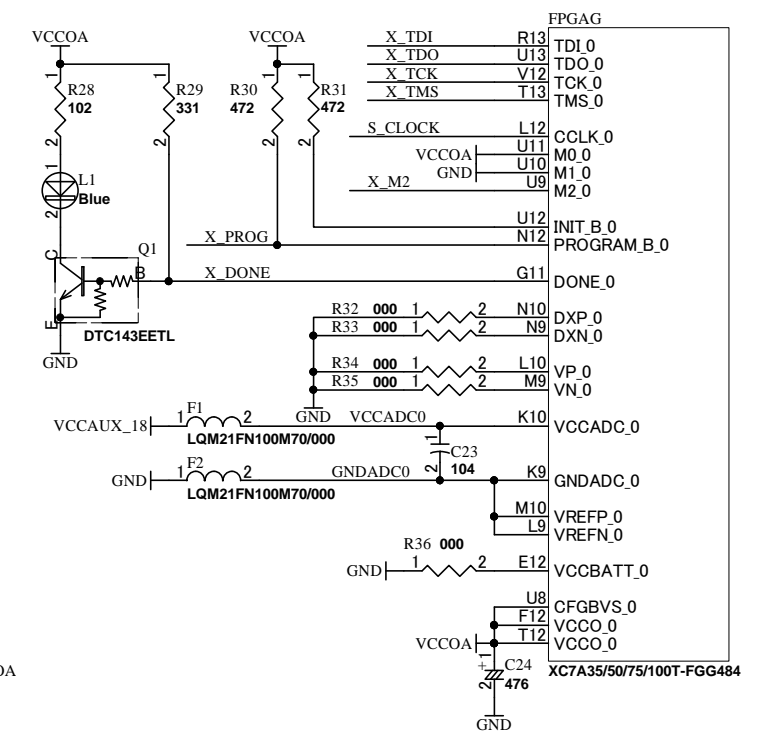
FPGA	
X AA16	IO L1P_T0_13
X AB18	IO L1N_T0_13
X AB19	IO L2P_T0_13
X AB13	IO L2N_T0_13
X AA13	IO L3P_T0_DQS_13
X AB13	IO L3N_T0_DQS_13
X AA13	IO L4P_T0_13
X AB13	IO L4N_T0_13
X AA14	IO L5P_T0_13
X AA14	IO L5N_T0_13
X W14	IO L6P_T0_13
X Y14	IO L6N_T0_VREF_13
X AB11	IO L7P_T1_13
X AB12	IO L7N_T1_13
X AA9	IO L8P_T1_13
X AB10	IO L8N_T1_13
X AA10	IO L9P_T1_DQS_13
X AA11	IO L9N_T1_DQS_13
X V10	IO L10P_T1_13
X W10	IO L10N_T1_13
X Y11	IO L11P_T1_SRCC_13
X Y12	IO L11N_T1_SRCC_13
X W11	IO L12P_T1_MRCC_13
X W12	IO L12N_T1_MRCC_13
X V13	IO L13P_T2_MRCC_13
X V14	IO L13N_T2_MRCC_13
X U15	IO L14P_T2_SRCC_13
X V15	IO L14N_T2_SRCC_13
X T14	IO L15P_T2_DQS_13
X T15	IO L15N_T2_DQS_13
X W15	IO L16P_T2_13
X T16	IO L16N_T2_13
X U16	IO L17P_T2_13
X U16	IO L17N_T2_13
X Y17	IO_0_13

VCCOA	
RJ3	(Disable)
(Enable)	
GND	

FPGA	
S_D0	P22
S_D1	R22
S_D2	P21
S_D3	R21
X_PUDC	U22
X_V22	
X T21	
X U21	
X P19	
X R19	
X T19	
X T20	
X W21	
X W22	
X AA20	
X AA21	
X Y21	
X Y22	
X U20	
X V20	
X W19	
X W20	
X Y18	
X Y19	
X V18	
X V19	
X AA19	
X AB20	
X V17	
X W17	
X AA18	
X AB18	
X U17	
X U18	
X P14	
X R14	
X R18	
X T18	
X N17	
X P17	
X P15	
X R16	
X N13	
X N14	
X P16	
X R17	
X P20	
X N15	

FPGA	
ULED2	H13
ULED3	G13
IOA33	G19
IOA32	G16
IOA35	J19
IOA34	H14
IOA6	G17
IOA7	G18
IOA37	J19
IOA36	H15
IOA8	H17
IOA9	H18
IOA11	J22
IOA10	H22
IOA12	H20
IOA13	G20
IOA24	K21
IOA25	K22
X M21	
X J21	
X J20	
X J19	
X H19	
X K18	
X K19	
X L19	
X L20	
X N22	
X M22	
X M18	
X L18	
X N18	
X N19	
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X M20	
X K13	
X K14	
X M13	
X L13	
X K17	
X L17	
X L14	
X L15	
X L16	
X K16	
X M15	
X M16	
X J16	IO_0_15
X M17	IO_25_15



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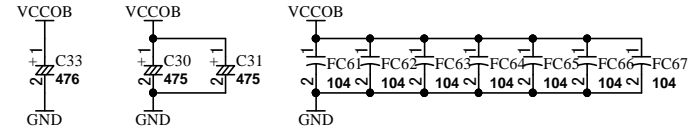
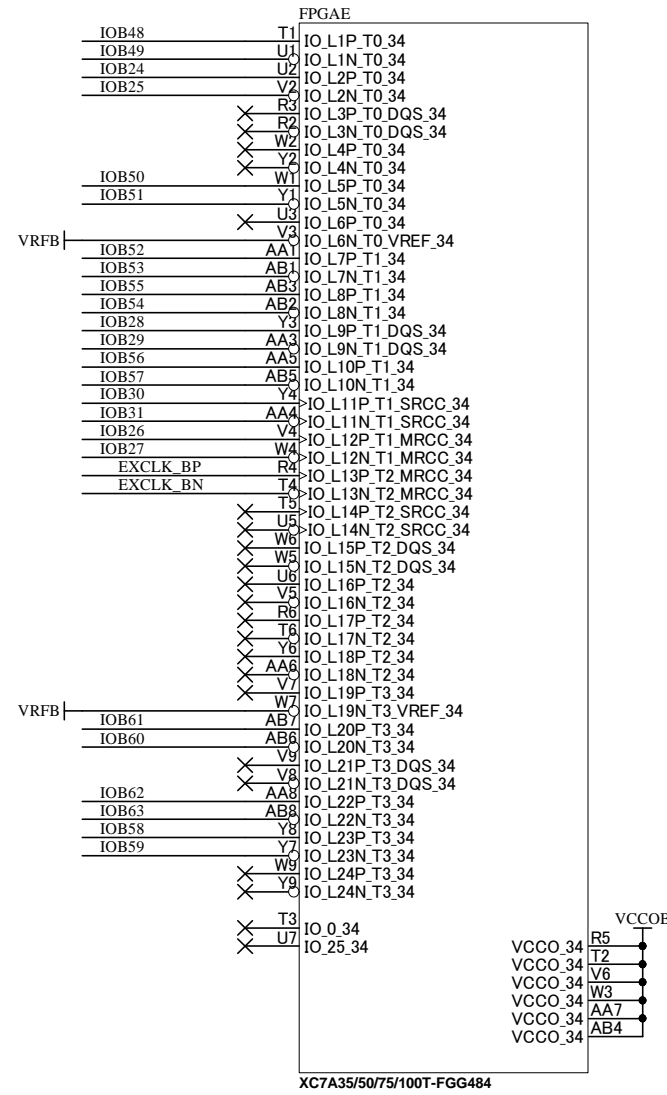
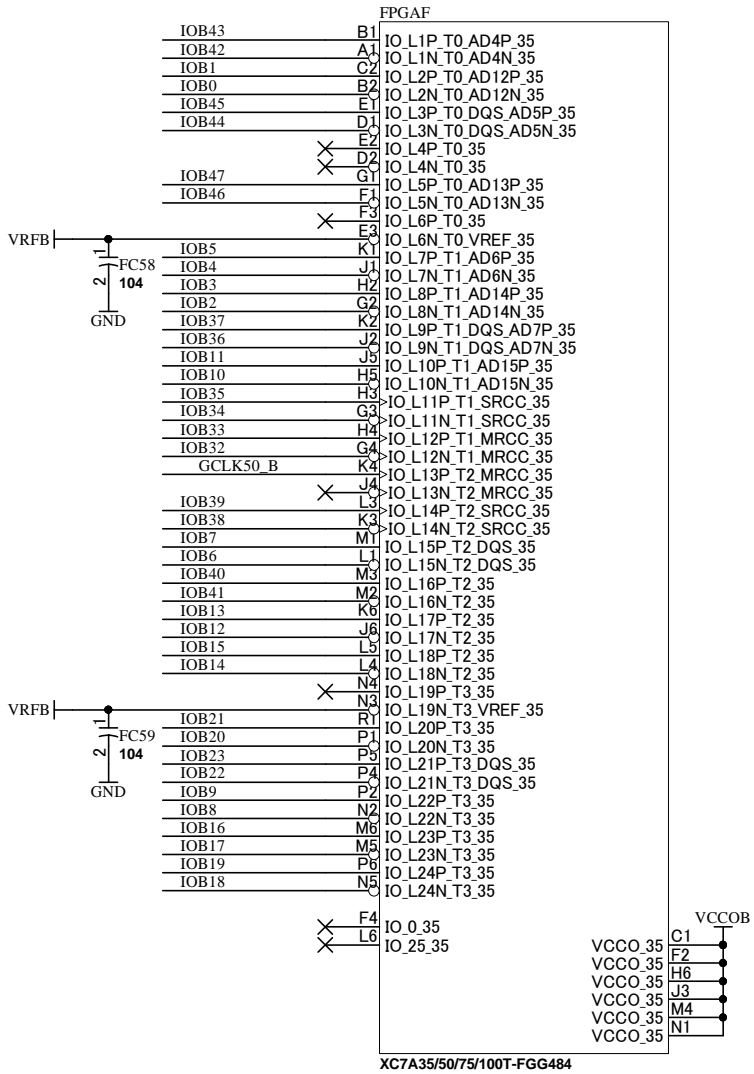
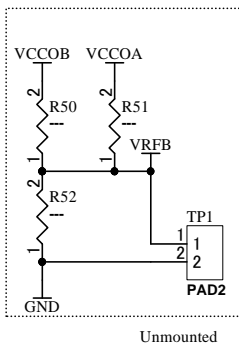
DOC. No. XCM-114      A

Date: 2014/10/30      10:26:09      File: IOA\_CONFIG.sch      Sheet 4 of 7

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V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VCCAUX_18	VCCAUX_18
VMGTAVTT_12	VMGTAVTT_12
VMGTVCC_10	VMGTVCC_10
VMGTCLK	VMGTCLK
VDDR	VDDR
VCCOB	VCCOB
VCCOA	VCCOA
GND	GND

IOB[0..63]	IOB[0..63]
GCLK50_B	GCLK50_B
EXCLK_BP	EXCLK_BP
EXCLK_BN	EXCLK_BN

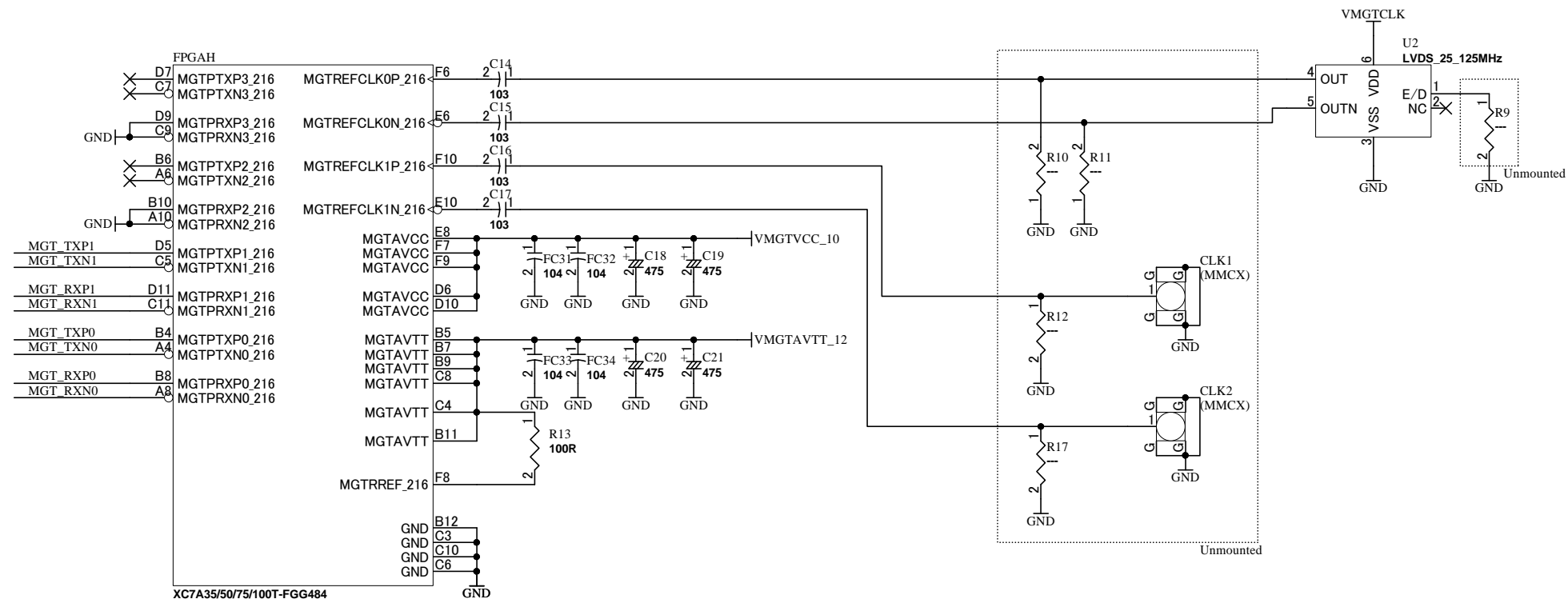


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V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VCCAUX_18	VCCAUX_18
VMGTAVTT_12	VMGTAVTT_12
VMGTVCC_10	VMGTVCC_10
VMGTCLK	VMGTCLK
VDDR	VDDR
VCCOB	VCCOB
VCCOA	VCCOA
GND	GND

MGT_TXP[0..1]	MGT_TXP[0..1]
MGT_TXN[0..1]	MGT_TXN[0..1]
MGT_RXP[0..1]	MGT_RXP[0..1]
MGT_RXN[0..1]	MGT_RXN[0..1]



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