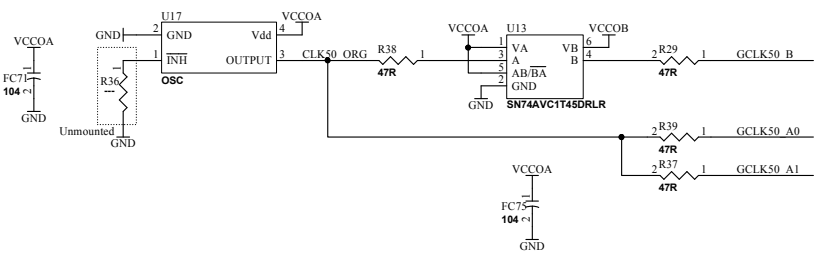
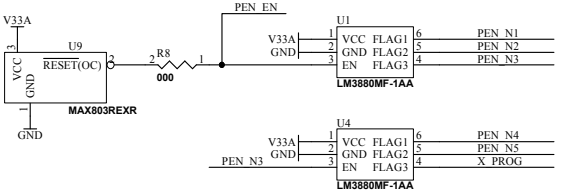
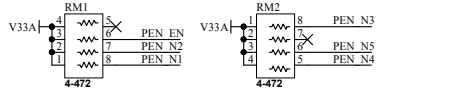
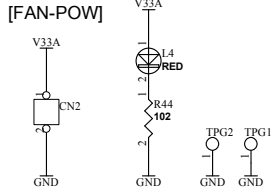
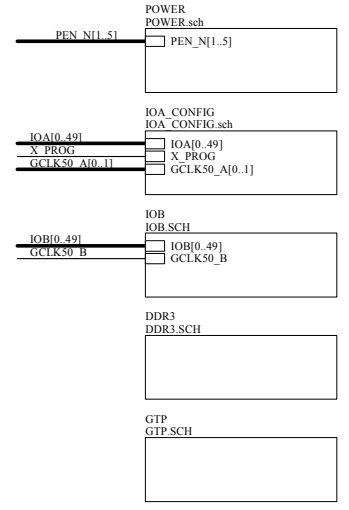
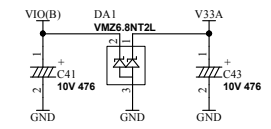


V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVCC_10	VMGTAVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VMGTCLK	VMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND

[POWER]



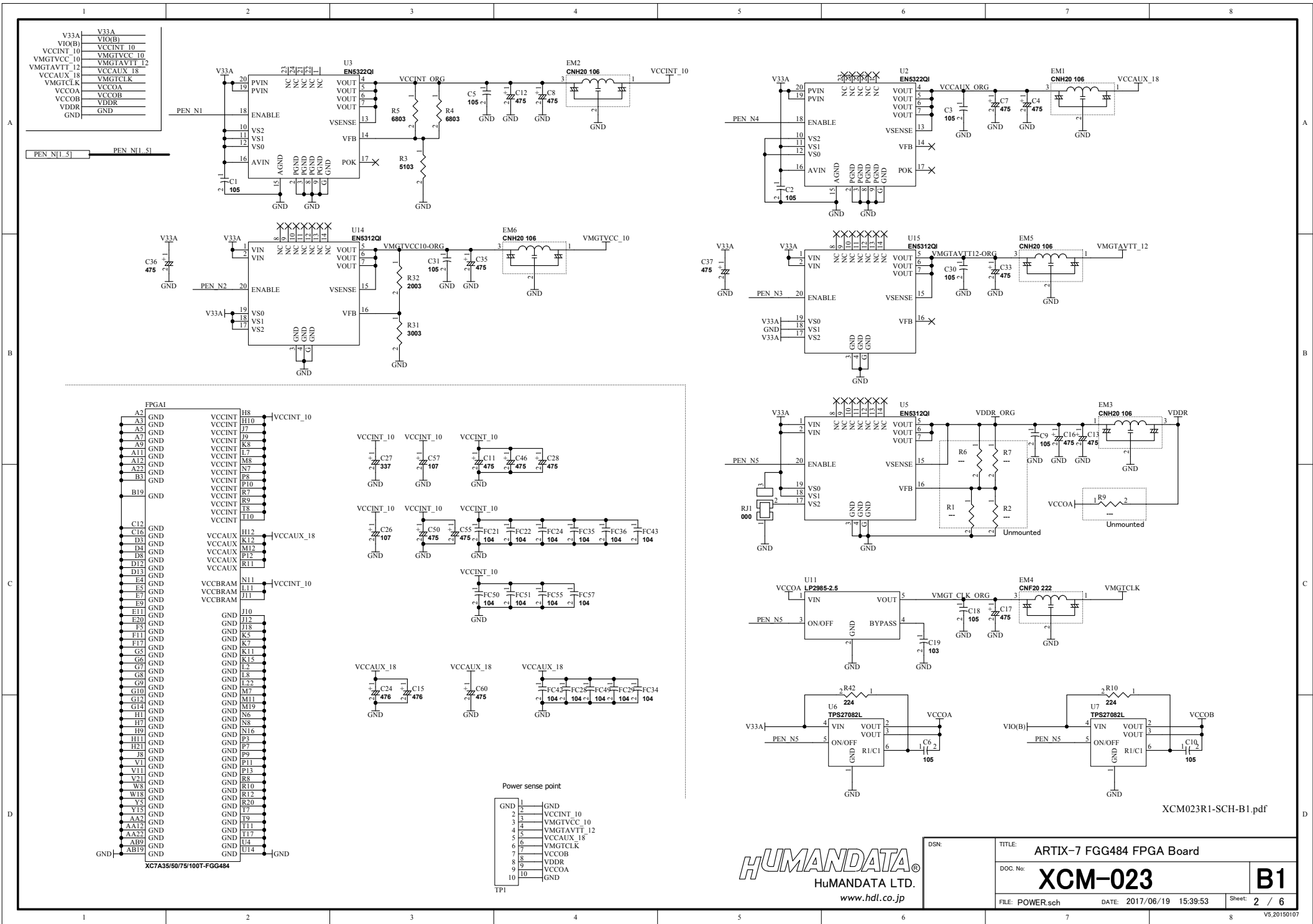
CNA		CNB	
V33A	VIO(A)	VIO(B)	VIO(B)
X	5V	X	5V
X	5V	X	5V
GND	GND	GND	GND
GND	GND	GND	GND
IOA0	IOB0		
IOA1	IOB1		
IOA2	IOB2		
IOA3	IOB3		
IOA4	IOB4		
IOA5	IOB5		
IOA6	IOB6		
IOA7	IOB7		
IOA8	IOB8		
GND	GND		
GND	GND		
IOA9	IOB9		
IOA10	IOB10		
IOA11	IOB11		
IOA12	IOB12		
IOA13	IOB13		
IOA14	IOB14		
IOA15	IOB15		
GND	GND		
GND	GND		
IOA16	IOB16		
IOA17	IOB17		
IOA18	IOB18		
IOA19	IOB19		
IOA20	IOB20		
IOA21	IOB21		
IOA22	IOB22		
IOA23	IOB23		
GND	GND		
GND	GND		
IOA24	IOB24		
IOA25	IOB25		
IOA26	IOB26		
IOA27	IOB27		
IOA28	IOB28		
IOA29	IOB29		
IOA30	IOB30		
IOA31	IOB31		
GND	GND		
GND	GND		
IOA32	IOB32		
IOA33	IOB33		
IOA34	IOB34		
IOA35	IOB35		
IOA36	IOB36		
IOA37	IOB37		
IOA38	IOB38		
IOA39	IOB39		
GND	GND		
GND	GND		
IOA40	IOB40		
IOA41	IOB41		
IOA42	IOB42		
IOA43	IOB43		
IOA44	IOB44		
IOA45	IOB45		
IOA46	IOB46		
IOA47	IOB47		
IOA48	IOB48		
IOA49	IOB49		
GND	GND		
GND	GND		



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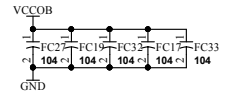
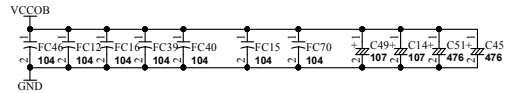
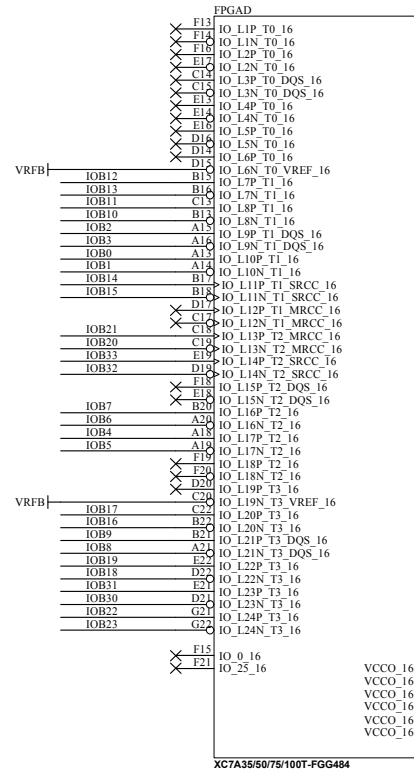
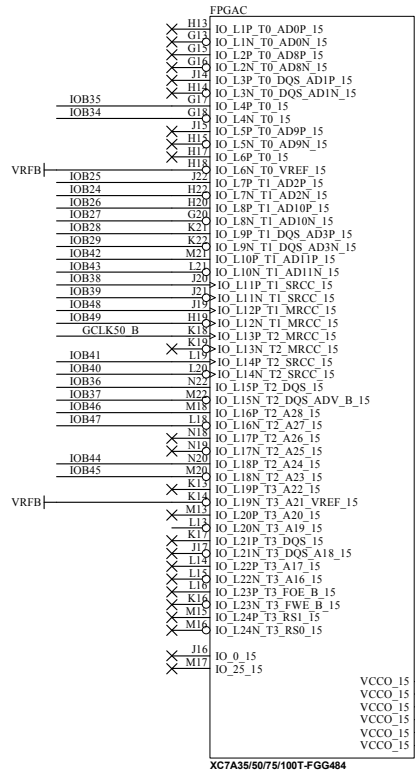
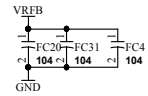
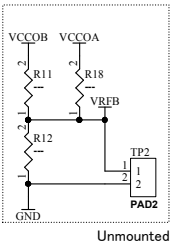
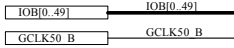
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DOC. No:	XCM-023
FILE: XCM023B.sch	DATE: 2017/06/19 15:39:53
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V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVCC_10	VMGTAVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VMGTCLK	VMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND

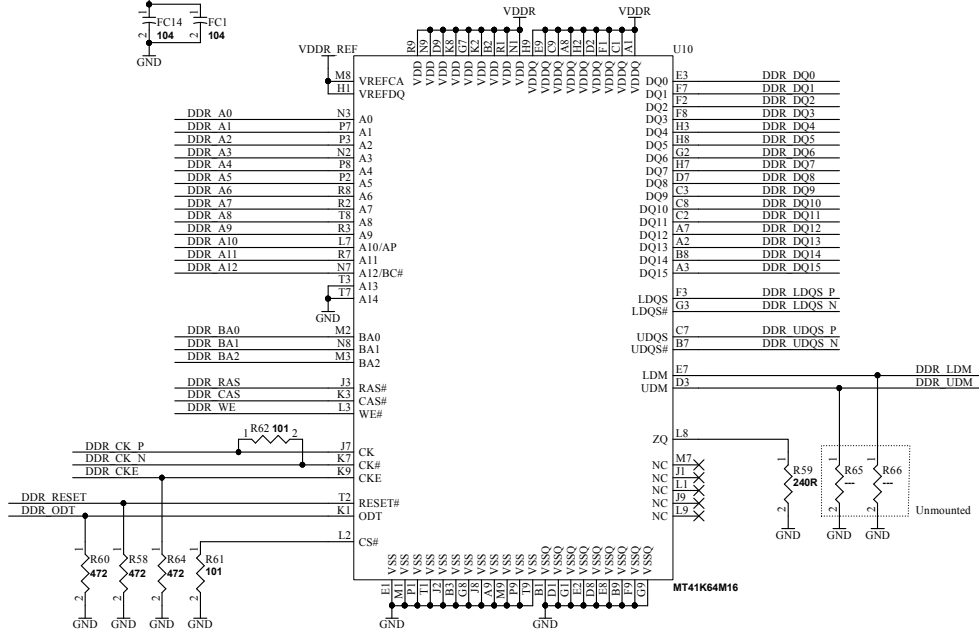
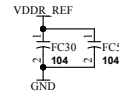
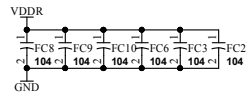
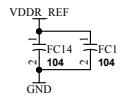
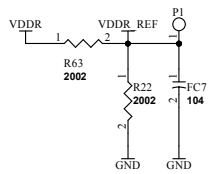


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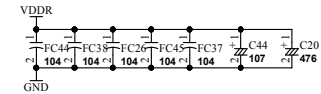


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DOC. No: XCM-023	B1
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Sheet: 4 / 6	V5_20150107

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVCC_10	VMGTAVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VCMGTCLK	VCMGTCLK
VCCOA	VCCOA
VCCOB	VCCOB
VDDR	VDDR
GND	GND



FPGA	
DDR DQ6	T1
DDR DQ4	U1
DDR DQ0	U1
DDR DQ7	V7
DDR LDQS P	R3
DDR LDQS N	R1
DDR DQ1	W1
DDR LDM	V2
DDR DQ5	W1
DDR DQ3	Y1
DDR DQ2	U1
V3	V3
DDR DO11	AA
DDR DQ9	AB
DDR DQ8	AB
DDR UDM	AB
DDR UDQS P	Y1
DDR UDQS N	AA
DDR DQ14	AA
DDR DQ10	AB
DDR DQ13	Y4
DDR DQ12	AA
DDR DQ15	Y1
DDR RESET	W1
DDR CKE	R1
DDR CAS	T1
DDR A3	T1
DDR BA2	U1
DDR ODT	W1
DDR WE	W1
DDR A5	U1
DDR BA0	V1
DDR A7	R1
DDR A2	T1
DDR A10	Y1
DDR A6	AA
DDR A12	W1
DDR A11	AB
DDR A8	AB
DDR CK P	V1
DDR CK N	V1
DDR A1	AA
DDR BA1	AB
DDR RAS	Y1
DDR A4	Y1
DDR A0	W1
DDR A9	Y1
IO 0_34	T3
IO 25_34	U7
VCCO_34	R5
VCCO_34	T2
VCCO_34	V6
VCCO_34	W3
VCCO_34	AA7
VCCO_34	AB4

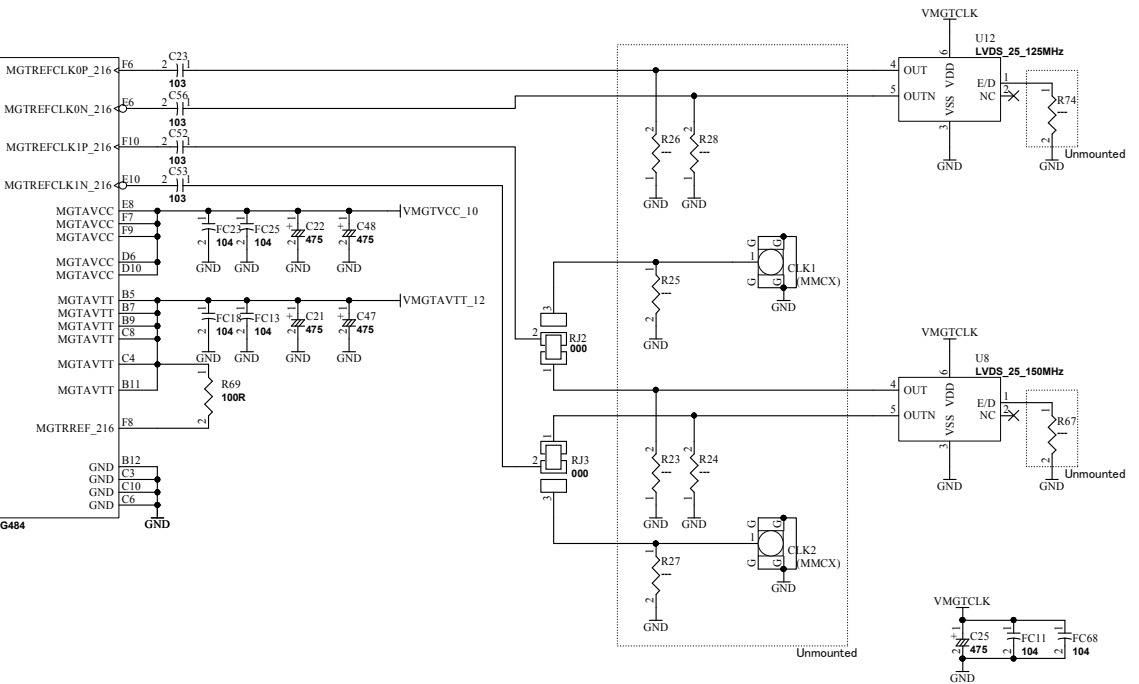
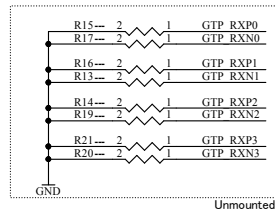
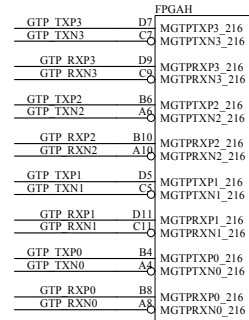
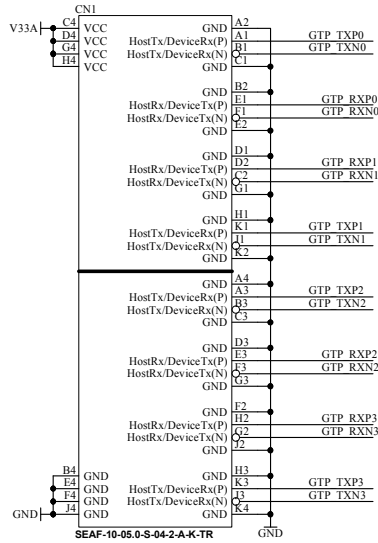


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DSN:	TITLE: ARTIX-7 FGG484 FPGA Board	B1
DOC. No:	XCM-023	
FILE: DDR3.SCH	DATE: 2017/06/19 15:39:54	Sheet: 5 / 6

V33A	V33A
VIO(B)	VIO(B)
VCCINT_10	VCCINT_10
VMGTAVCC_10	VMGTAVCC_10
VMGTAVTT_12	VMGTAVTT_12
VCCAUX_18	VCCAUX_18
VCCCLK	VCCCLK
VCCDA	VCCDA
VCCOB	VCCOB
VDDR	VDDR
GND	GND

SIF40 (Receptacle)



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DSN:	TITLE: ARTIX-7 FGG484 FPGA Board
DOC. No:	XCM-023
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Sheet: 6 / 6	B1