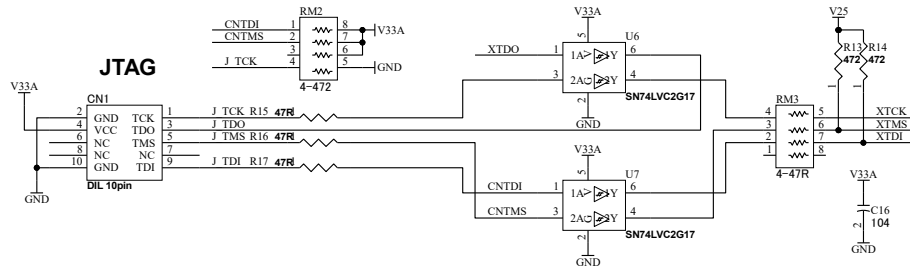
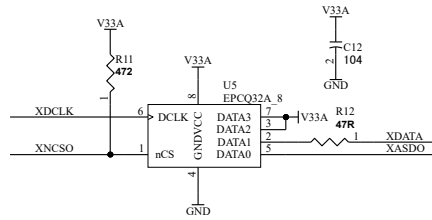
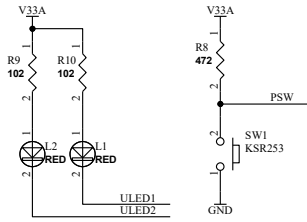
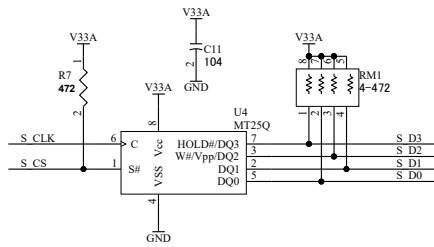
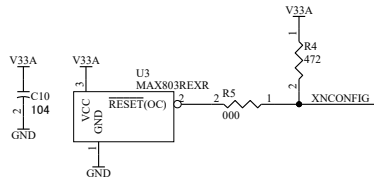
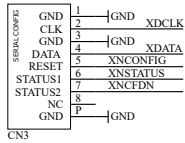
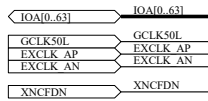


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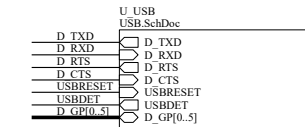
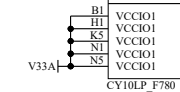
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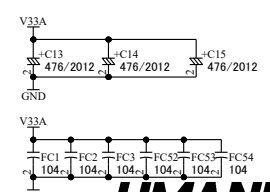


FPGA	
EXCLK AN	A14
EXCLK AP	B14
IOA41	C5
IOA40	D5
IOA24	C13
IOA25	D13
IOA30	C14
IOA31	D14
IOA28	C12
IOA29	D12
IOA19	A12
IOA18	B12
IOA27	F14
IOA26	E14
IOA17	A11
IOA16	B11
IOA15	A10
IOA14	B10
IOA60	G13
IOA61	H13
IOA51	C10
IOA50	D10
IOA62	E12
IOA63	F12
IOA57	E11
IOA56	F11
IOA11	A7
IOA10	B7
IOA9	A6
IOA8	B6
IOA59	C11
IOA58	D11
IOA49	C9
IOA48	D9
IOA13	A8
IOA12	B8
IOA47	C8
IOA46	D8
IOA45	C7
IOA44	D7
IOA43	E7
IOA55	E8
IOA54	F8
IOA52	E5
IOA53	F5
IOA7	A4
IOA6	B4
IOA4	B3
IOA5	A3
IOA39	C4
IOA38	D4
IOA42	D6
IOA23	E4
E10	IOB8(O080)
IOA43	C6
G14	IO_VREFB8N0/B8
G12	IO_VREFB8N1/B8
G9	IO_VREFB8N2/B8
A2	VCCIO8
A1	VCCIO8
A5	VCCIO8
A9	VCCIO8
A13	VCCIO8
E6	VCCIO8
E9	VCCIO8
E13	VCCIO8
H11	VCCIO8

FPGA	
GCLK50L	J2
GND	J1
IOA36	D3
IOA37	C2
IOA2	D2
IOA3	D1
IOA35	E3
IOA34	F3
IOA21	F5
XASDO	F4
IOA33	G4
IOA32	G3
XNCSO	E2
IOA1	E1
IOA0	F2
D TXD	J4
D RXD	J3
D GP0	G2
D GP1	G1
D CTS	K2
D RTS	K1
D GP3	K4
D GP2	K3
D GP4	M3
S_CLK	L2
S_CS	L1
S_D1	M2
S_D2	M1
S_D3	J2
S_D0	P1
IOA20	G5
IOA22	G6
	N4
	N3
PSW	H5
ULED1	H6
ULED2	H7
USBRESET	L5
USBDET	M5
	B1
	H1
	K5
	N1
	N5



### Bank Group A(3.3V)

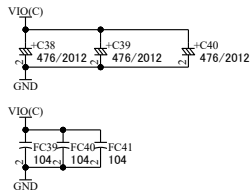
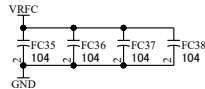
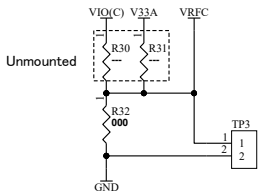
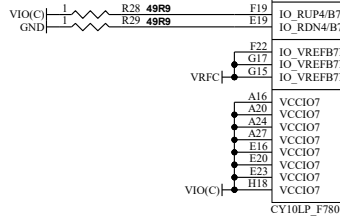
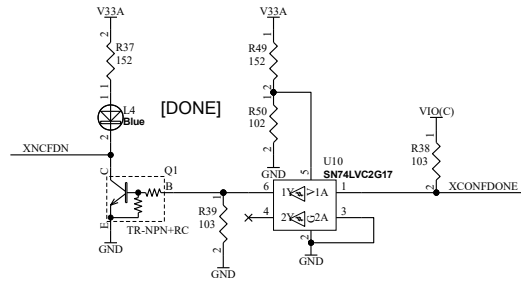
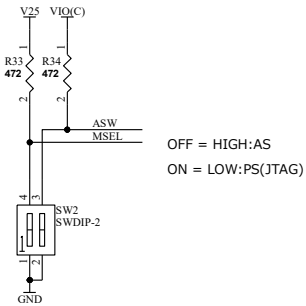


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IOCI0\_831  
 EXCLK C1P  
 EXCLK C1N  
 EXCLK C2P  
 EXCLK C2N  
 XNCFDN



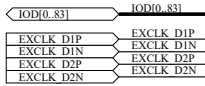
FPGA	
EXCLK C1N	A15
EXCLK C1P	B15
IOC32	C23
IOC33	D23
IOC65	C26
IOC64	B26
IOC57	D22
IOC56	E22
IOC13	A26
IOC12	A25
IOC30	E21
IOC31	F21
IOC67	D25
IOC66	C25
IOC10	A23
IOC11	B23
IOC60	C24
IOC61	D24
IOC55	C22
IOC54	D21
IOC8	A22
IOC9	B22
IOC6	A21
IOC7	E18
IOC62	E18
IOC63	F18
IOC49	C18
IOC48	D18
IOC53	C20
IOC52	D20
IOC51	C19
IOC50	D19
IOC47	C17
IOC46	D17
IOC4	A19
IOC5	B19
IOC2	A18
IOC3	B18
IOC59	E25
IOC58	E24
IOC45	C16
IOC44	D16
IOC1	A17
IOC1	B17
IOC42	C15
IOC43	D15
F15	
G16	
F17	
G18	
G18	
B25	
C21	
E17	
E15	
F19	
E19	
F22	
G17	
G15	
A16	VCCIO7
A20	VCCIO7
A24	VCCIO7
A27	VCCIO7
E16	VCCIO7
E20	VCCIO7
E23	VCCIO7
H18	VCCIO7
CY10LP_F780	

FPGA	
EXCLK C2N	J28
EXCLK C2P	J27
IOC80	P26
IOC81	P25
IOC29	P28
IOC28	P27
IOC78	N26
IOC79	N25
IOC27	M28
IOC26	M27
IOC76	M26
IOC77	M25
IOC25	L28
IOC24	L27
IOC83	L24
IOC82	L23
IOC23	K28
IOC22	K27
IOC75	J26
IOC74	J25
IOC21	G28
IOC20	G27
IOC41	K26
IOC40	K25
IOC19	K24
IOC18	F27
IOC17	E28
IOC16	E27
IOC71	F26
IOC70	F25
IOC73	H26
IOC72	H25
IOC15	D28
IOC14	D27
IOC34	C27
IOC35	D26
IOC37	H24
IOC36	H23
IOC39	C26
IOC38	C25
IOC69	F25
IOC68	F24
XCONF_DONE	P24
MSEL	N22
GND	P23
V25	M22
V25	P22
M24	IO/B6
L26	IO/B6
L25	IO/B6
N21	IO_VREFB0N/B6
M21	IO_VREFB0N/B6
J22	IO_VREFB0N/B6
B28	VCCIO6
H28	VCCIO6
K24	VCCIO6
N24	VCCIO6
N28	VCCIO6
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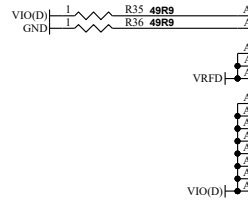
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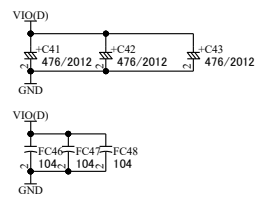
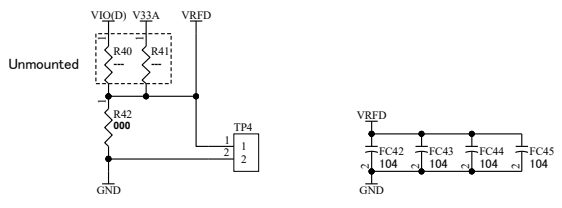
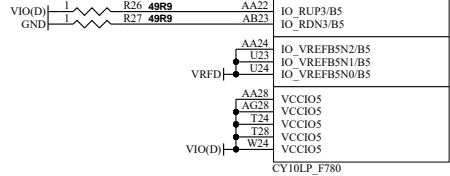
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FPGAF	
EXCLK D1P	AG15
EXCLK D1N	AH15
IOD13	AE23
IOD12	AF23
IOD2	AC15
IOD3	AD15
IOD74	AE15
IOD75	AF15
IOD43	AG17
IOD42	AH17
	AA16
	AB16
IOD76	AE17
IOD77	AF17
IOD45	AG18
IOD44	AH18
IOD47	AG19
IOD46	AH19
IOD30	AC17
IOD1	AD17
IOD49	AG21
IOD48	AH21
IOD79	AF18
IOD78	AF18
IOD51	AG22
IOD50	AH22
IOD53	AG23
IOD52	AH23
IOD5	AF19
IOD4	AF19
IOD14	AF24
IOD15	AF25
IOD7	AE20
IOD6	AF20
IOD9	AE21
IOD8	AF21
IOD16	AE25
IOD17	AE26
IOD55	AG25
IOD54	AH25
IOD11	AE22
IOD10	AF22
IOD19	AD25
IOD18	AE24
IOD80	AC21
IOD81	AD21
IOD57	AG26
IOD56	AH26
	AF16
	AE16
	Y19
	AD18
	AD24
	AA17
	AB17
	AA15
	AC18
	AB20
	AA18
	AD16
	AD30
	AD23
	AH16
	AH20
	AH24
	AH27



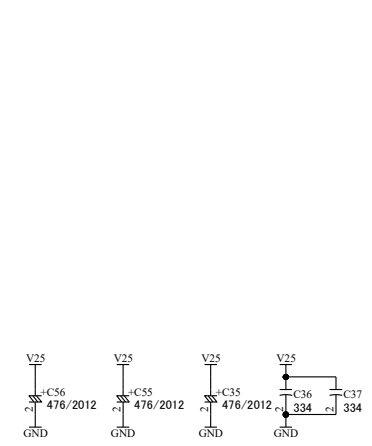
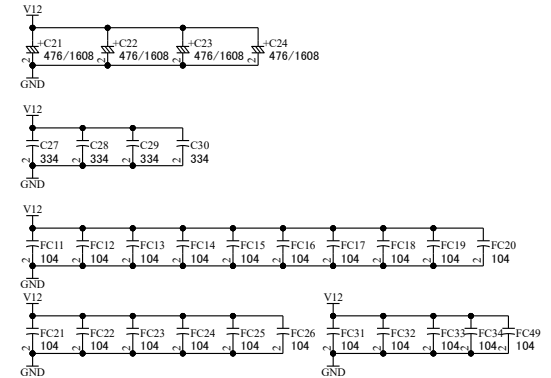
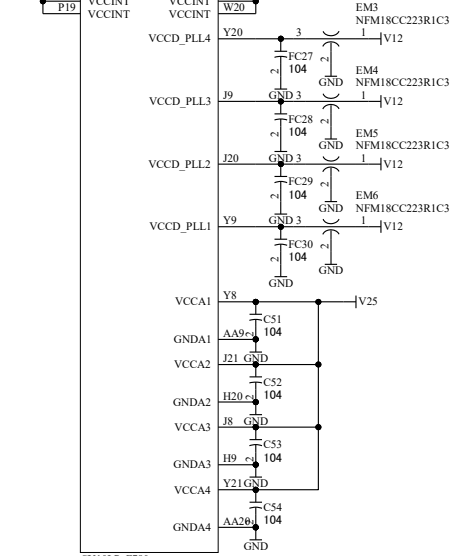
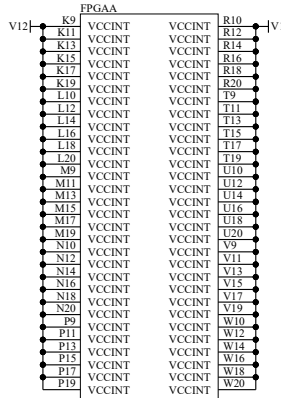
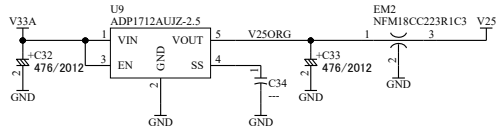
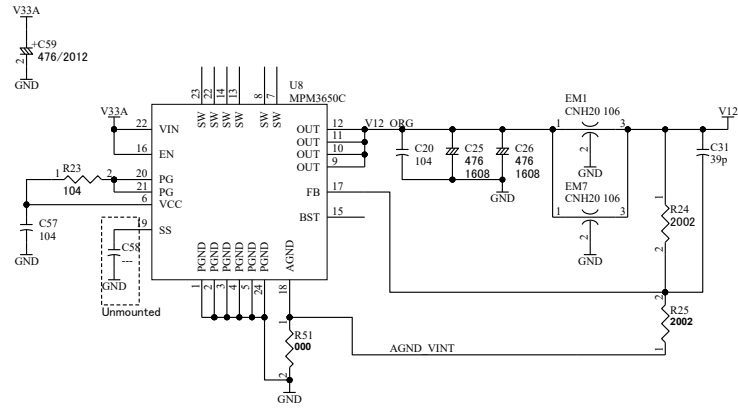
FPGAK	
EXCLK D2N	Y28
EXCLK D2P	Y27
IOD83	AC25
IOD82	AC24
IOD20	AD26
IOD21	AC26
IOD59	AE28
IOD58	AE27
IOD61	AD28
IOD60	AD27
IOD39	Y24
IOD38	Y23
IOD63	AC28
IOD62	AC27
IOD23	AB26
IOD22	AB25
IOD25	AA26
IOD24	AA25
IOD65	AB28
IOD64	AB27
IOD26	Y26
IOD27	Y25
IOD28	W26
IOD29	W25
IOD66	W27
IOD67	W28
IOD69	V28
IOD68	V27
IOD30	V26
IOD31	V25
IOD41	V24
IOD40	V23
IOD70	U27
IOD71	U28
IOD32	U26
IOD33	U25
	T26
	T25
	T22
	T21
	T20
	R26
	R25
	R28
	R27
	AB24
	R24
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	AA24
	U23
	U24
	AA28
	AC28
	T24
	T28
	W24



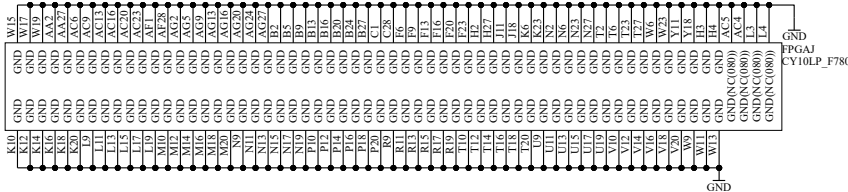
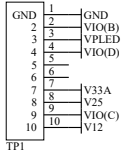
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