

ACM-20-XX SDRAM 設定例

SDRAM Controller - sdram_0

Presets: (Custom)

Memory Profile | Timing

Data Width: 16 Bits

Architecture: Chip Selects: 1 Banks: 4

Address Widths: Row: 13 Column: 9

Share Pins via Tristate Bridge: Controller shares dq/dqm/addr I/O pins.

Generic Memory Model (Simulation Only): Include a functional memory model in the system testbench.

Memory size: 32 MBytes
16777216 x 16
256 Mbits

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SDRAM Timing Parameters

CAS latency cycles: 1

Initialization refresh cycles: 2

Issue one refresh command every: 15.625 us

Delay after powerup, before initialization: 100 us

Duration of refresh command (t_{rfc}): 70 ns

Duration of precharge command (t_{rp}): 20 ns

ACTIVE to READ or WRITE delay (t_{rcd}): 20 ns

Access time (t_{ac}): 55 ns

Write recovery time (t_{wr}, No auto precharge): 14 ns

ACM-20-XX SPI ROM 設定例

SPI - spi_0

Master/Slave: Slave Master

Generate: 1 select (SS_n) signals. One for each slave.

SPI Clock (SCLK) Rate: 10 MHz

Actual Rate = 7.5MHz Error: -25%

Actual Delay = 333ns

Specify Delay: 300 ns

Delay granularity (1/2 SCK) = 66.666ns

Data Register: Width: 8 bits

Shift direction: MSB first LSB first

Timing: Clock Polarity: 0 1

Clock Phase: 0 1

Waveforms: SS_n, SCLK 333ns, MOSI (MSB, LSB)

SRAM 設定例

Interface to User Logic - ext_ram

Ports | Instantiation | Timing | Publish

Bus Interface Type: Avalon Memory Slave

Design Files: Import Verilog, VHDL, EDIF, or Quartus Schematic File

Top module: []

| Port Name | Width | Direction | Shared | Type |
|--------------|-------|-----------|-------------------------------------|----------------|
| address | 16 | input | <input type="checkbox"/> | address |
| write_n | 1 | input | <input type="checkbox"/> | write_n |
| read_n | 1 | input | <input type="checkbox"/> | outputenable_n |
| data | 16 | inout | <input checked="" type="checkbox"/> | data |
| chipselect_n | 1 | input | <input checked="" type="checkbox"/> | chipselect_n |
| byteenable_n | 2 | input | <input type="checkbox"/> | byteenable_n |

Interface to User Logic - ext_ram

Ports | Instantiation | Timing | Publish

Do not simulate user logic (An empty module will be inserted instead).

Simulate user logic (Imported HDL will be simulated with the system).

Export Bus Ports (You must manually connect every port correctly).

System Module

User Logic

Interface to User Logic - ext_ram

Ports | Instantiation | Timing | Publish

Setup: 40 Wait: 20 Hold: 20 Units: ns

System Clock 30 MHz Timing granularity is System Clock cycles.

Read Waveforms: data, addr, select, readn 66ns 33ns

Write Waveforms: data, addr, select, writen 66ns 33ns 33ns