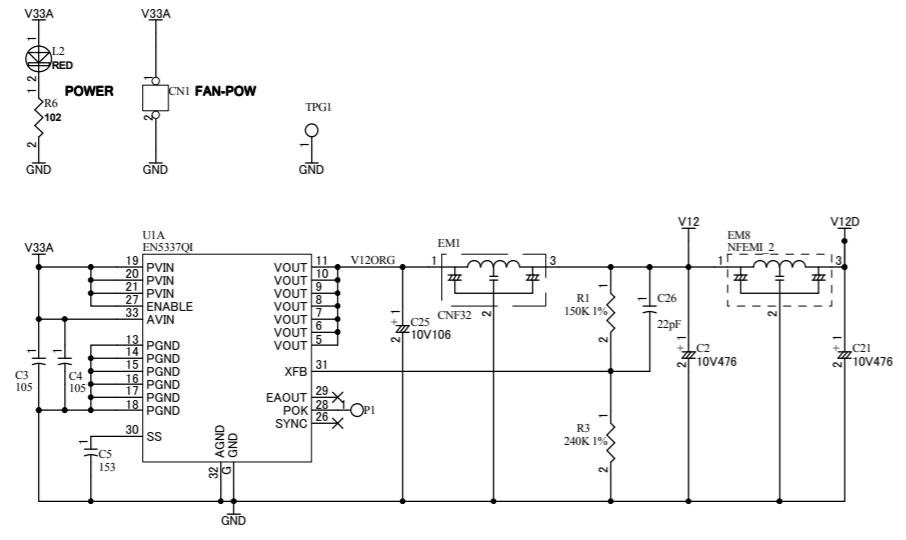
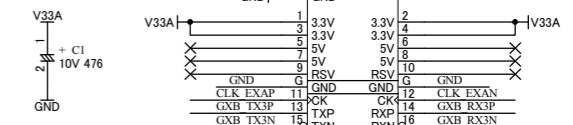
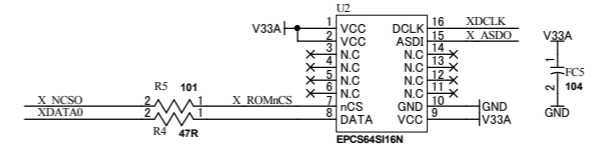
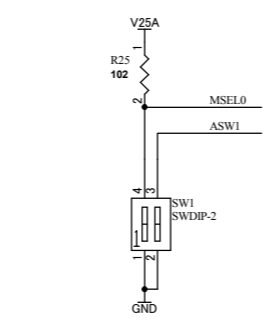


V33A	V33A
VIO(B)	V25
V25A	V25A
V25GXB	V25GXB
V12	V12D
V12GXB	V12GXB
V18	V18
V09REF	V09REF
VSB1	VSB2
VREFB	VREFB
GND	GND

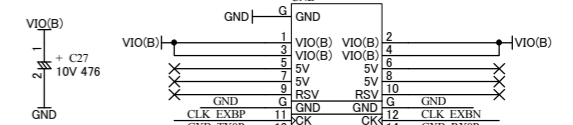
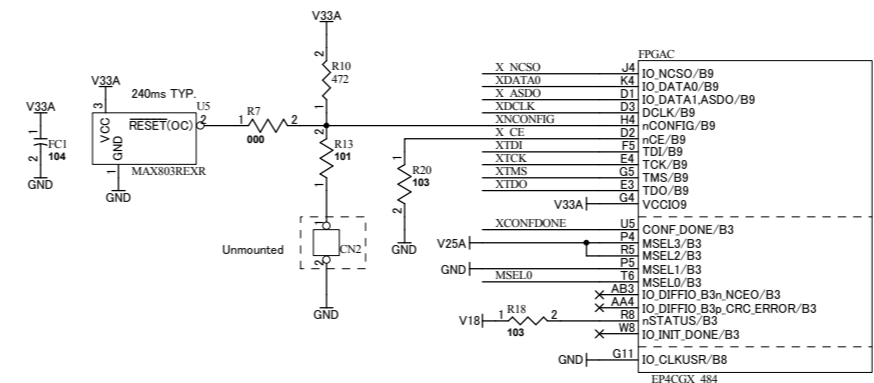
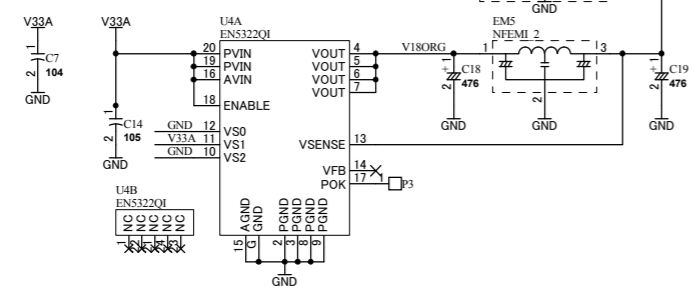
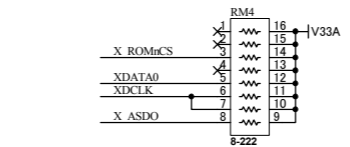
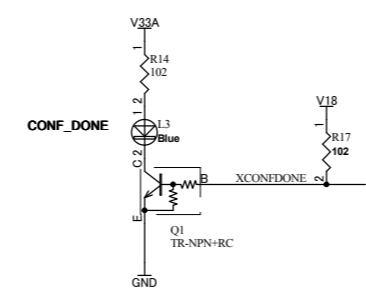
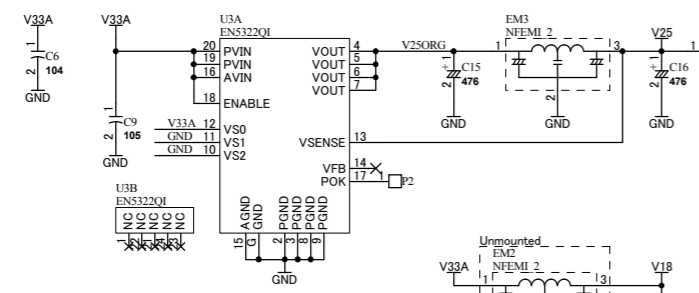


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NC/SW	79
NC/SW	80



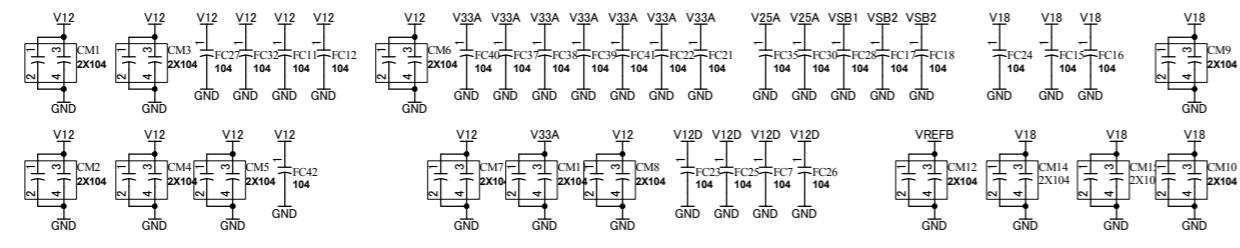
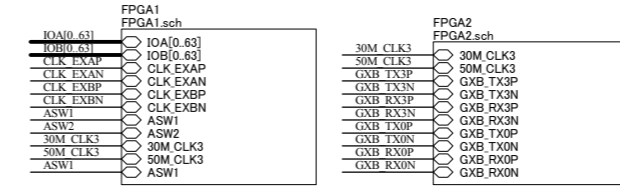
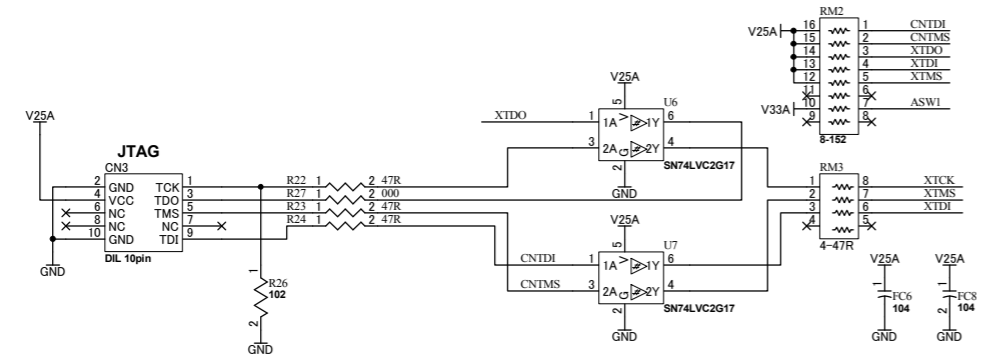
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V33A	7	5V	8
V33A	8	5V	9
V33A	9	RSV	10
V33A	10	RSV	11
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V33A	13	RSV	14
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V33A	39	RSV	40
V33A	40	RSV	41
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V33A	64	RSV	65
V33A	65	RSV	66
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V33A	68	RSV	69
V33A	69	RSV	70
V33A	70	RSV	71
V33A	71	RSV	72
V33A	72	RSV	73
V33A	73	RSV	74
V33A	74	RSV	75
V33A	75	RSV	76
V33A	76	RSV	77
V33A	77	RSV	78
V33A	78	RSV	79
V33A	79	RSV	80

Bank Group A



GND	1	GND	2
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VIO(B)	5	VIO(B)	6
VIO(B)	6	VIO(B)	7
VIO(B)	7	VIO(B)	8
VIO(B)	8	VIO(B)	9
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VIO(B)	10	VIO(B)	11
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VIO(B)	12	VIO(B)	13
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VIO(B)	14	VIO(B)	15
VIO(B)	15	VIO(B)	16
VIO(B)	16	VIO(B)	17
VIO(B)	17	VIO(B)	18
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VIO(B)	32	VIO(B)	33
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VIO(B)	35	VIO(B)	36
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VIO(B)	78	VIO(B)	79
VIO(B)	79	VIO(B)	80

Bank Group B



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DOC. No. ACM-108

File: ACM108C.sch

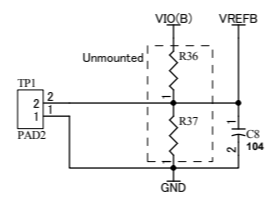
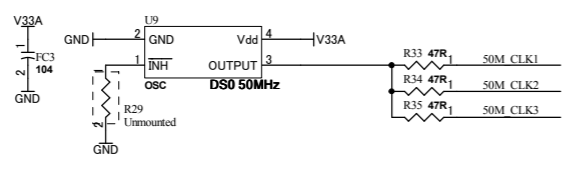
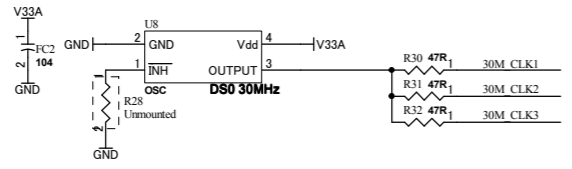
Sheet 1 of 3

ACM108R2-SCH-C

C

V33A	V33A	IOA0_63	IOA0_63
VIO(B)	VIO(B)	IOB0_63	IOB0_63
V25	V25	ASW1	ASW1
V25A	V25A	ASW2	ASW2
V25GXB	V25GXB		
V12	V12		
V12GXB	V12GXB		
V18	V18		
V09REF	V09REF		
VSB1	VSB1		
VSB2	VSB2		
VREFB	VREFB		
GND	GND		

CLK EXAP	CLK EXAP
CLK EXAN	CLK EXAN
CLK EXBP	CLK EXBP
CLK EXBN	CLK EXBN
30M CLK3	30M CLK3
50M CLK3	50M CLK3
ASW1	ASW1



FPGA F	
CLK_EXBN	M22
CLK_EXBP	M21
IOB33	R17
IOB32	R16
IOB59	W22
IOB58	W22
IOB37	W21
IOB36	W20
IOB39	V21
IOB38	V20
IOB40	U20
IOB41	T19
IOB35	T20
IOB34	R19
IOB61	U22
IOB60	V22
IOB43	R21
IOB42	R20
IOB63	T22
IOB62	T21
IOB13	L15
IOB12	P22
IOB4	R22
IOB5	M17
IOB9	L13
IOB8	M13
IOB1	N20
IOB10	N19
IOB7	N21
IOB6	M18
IOB54	T17
IOB55	T18
IOB54	R39
IOB55	R40
IOB54	U18
IOB55	P20
IOB54	M20
IOB55	N18
IOB54	P19
IOB55	R18
IOB54	VCCIO5
IOB55	VCCIO5
IOB54	VCCIO5
IOB55	VCCIO5

FPGA G	
30M_CLK1	L22
30M_CLK1	L21
IOB3	L20
IOB2	L19
IOB45	J20
IOB44	J19
IOB53	K22
IOB50	J21
IOB49	J22
IOB48	K22
IOB1	K20
IOB0	K19
IOB47	H21
IOB46	H20
IOB52	G21
IOB53	G20
IOB16	F20
IOB17	F20
IOB21	F22
IOB30	G22
IOB18	E21
IOB23	D22
IOB22	D21
IOB29	B22
IOB28	C22
IOB30	A22
IOB31	A21
IOB15	D20
IOB14	D19
IOB27	A20
IOB26	B19
IOB56	C20
IOB57	C19
IOB25	B21
IOB24	B17
IOB54	G16
IOB55	G15
IOB54	F18
IOB55	F17
IOB54	J15
IOB55	H17
IOB54	G18
IOB55	G18
IOB54	H19
IOB55	J18
IOB54	K18
IOB55	K18

RIGHT EDGE IBANK 5/6 for Bank Group B

FPGA A	
F3	GND
M3	GND
T4	GND
U3	GND
V19	GND
E19	GND
H5	GND
AA11	GND
AA14	GND
AA17	GND
AA5	GND
AA8	GND
B1	GND
B14	GND
B17	GND
B2	GND
B5	GND
B8	GND
C21	GND
D18	GND
E7	GND
F11	GND
F13	GND
F15	GND
F21	GND
F9	GND
H11	GND
H18	GND
J6	GND
K1	GND
K15	GND
K21	GND
K9	GND
K7	GND
K9	GND
K9	GND
L10	GND
L12	GND
L18	GND
L6	GND
L8	GND
M5	GND
M9	GND
N10	GND
N4	GND
N6	GND
P16	GND
P18	GND
P21	GND
P9	GND
R12	GND
R6	GND
U10	GND
U17	GND
U21	GND
V11	GND
V14	GND
V8	GND
V5	GND
Y21	GND
AA1	GND
AA2	GND
AB1	GND
E1	GND
E2	GND
G1	GND
G2	GND
J1	GND
J2	GND
L1	GND
L2	GND
N1	GND
R1	GND
R2	GND
U1	GND
W1	GND
W2	GND

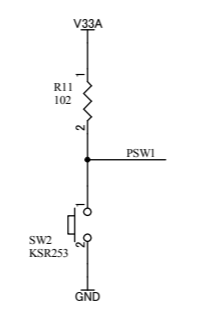
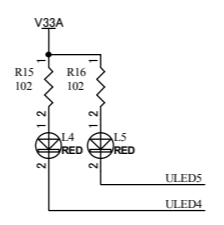
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VCCINT	E7
VCCINT	G13
VCCINT	G9
VCCINT	J11
VCCINT	J17
VCCINT	J17
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VCCINT	J9
VCCINT	K18
VCCINT	K6
VCCINT	K8
VCCINT	L1
VCCINT	L5
VCCINT	L7
VCCINT	L9
VCCINT	M12
VCCINT	M6
VCCINT	N16
VCCINT	N5
VCCINT	N8
VCCINT	P12
VCCINT	P17
VCCINT	P8
VCCINT	R7
VCCINT	T10
VCCINT	T12
VCCINT	J16

VCCD_PLL	G3
VCCD_PLL	M4
VCCD_PLL	L4
VCCD_PLL	U4
VCCD_PLL	V18
VCCD_PLL	E18

VCCA	F4
VCCA	L4
VCCA	T5
VCCA	U4
VCCA	U19
VCCA	F19

VCCINT(110/150)/IO_DIFFIO_B4p/B3	P10
VCCINT(110/150)/IO_DIFFIO_B32p/B4	T15
VCCINT(110/150)/IO_DIFFIO_R36p/B5	N14
VCCINT(110/150)/IO_DIFFIO_R36n/B5	M15
VCCINT(110/150)/IO_DIFFIO_R46p/B5	K14
VCCINT(110/150)/IO_DIFFIO_R46n/B5	H16
VCCINT(110/150)/IO_DIFFIO_R36p/B6	K12
VCCINT(110/150)/IO_DIFFIO_T25p/B7	J12

GND(110/150)/IO_DIFFIO_B4n/B3	R10
GND(110/150)/IO_DIFFIO_B32n/B4	R15
GND(110/150)/IO_DIFFIO_R36n/B5	N13
GND(110/150)/IO_DIFFIO_R35n/B5	M14
GND(110/150)/IO_DIFFIO_R46n/B5	M16
GND(110/150)/IO_DIFFIO_R27p/B5	L16
GND(110/150)/IO_DIFFIO_R6n/B6	K17
GND(110/150)/IO_DIFFIO_R6p/B6	K15
GND(110/150)/IO_DIFFIO_R46p/B6	H15
GND(110/150)/IO_DIFFIO_R36p/B6	J12



TOP EDGE IBANK 7/8 for Bank Group A

FPGA I	
CLK_EXAN	J10
CLK_EXAP	K10
IOA15	G10
IOA14	H9
IOA13	A8
IOA12	B7
IOA6	A6
IOA7	A7
IOA8	A4
IOA9	A5
IOA2	A2
IOA3	A3
IOA4	B3
IOA5	B4
IOA10	B6
IOA11	C6
IOA1	A1
IOA0	B1
IOA18	C8
IOA19	D8
IOA32	C1
IOA33	C2
IOA42	C7
IOA43	C7
IOA34	C3
IOA35	C4
IOA36	E8
IOA37	D4
IOA38	D5
IOA39	E5
IOA20	C9
IOA21	D9
IOA40	D6
IOA41	E6
ULED5	E9
ULED4	G7
ULED5	H7
PSW1	F6
IOA60	D12
IOA61	D10
IOA60	E10
IOA61	F10
IOA60	F10
IOA61	F10

FPGA H	
50M_CLK3	A9
30M_CLK2	B9
IOA55	C17
IOA54	G18
IOA26	A18
IOA27	A19
IOA56	D17
IOA57	E17
IOA52	B16
IOA53	C16
IOA24	A16
IOA25	A17
IOA58	C15
IOA59	D15
IOA50	A15
IOA51	B15
IOA30	C14
IOA31	D14
IOA49	A13
IOA48	A14
IOA28	C12
IOA29	C13
IOA46	B12
IOA47	B13
IOA44	C11
IOA45	C10
IOA44	C11
IOA45	C10
IOA16	A11
IOA17	A12
IOA22	A10
IOA23	B10
IOA23	G12
IOA23	H12
IOA23	B18
IOA62	F16
IOA63	F17
IOA62	D16
IOA63	D13
IOA62	F12
IOA63	F12
IOA62	E13
IOA63	E14
IOA62	E15
IOA63	E16
IOA62	E17
IOA63	E17

HUMAN DATA

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B1

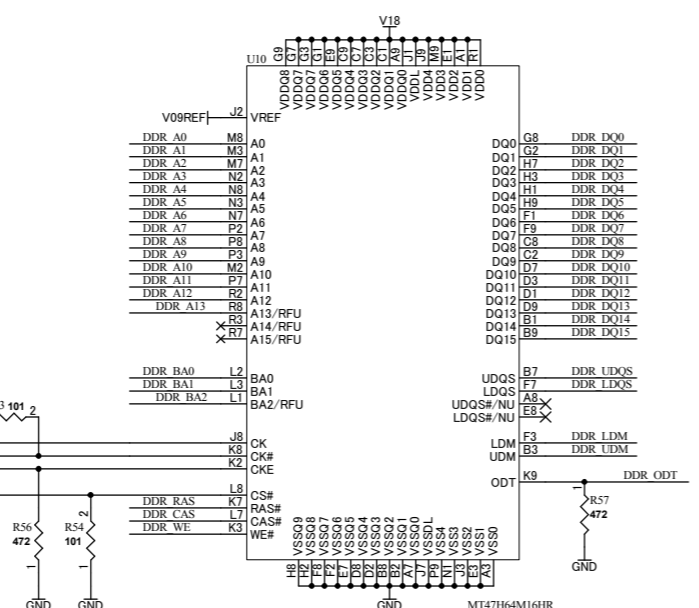
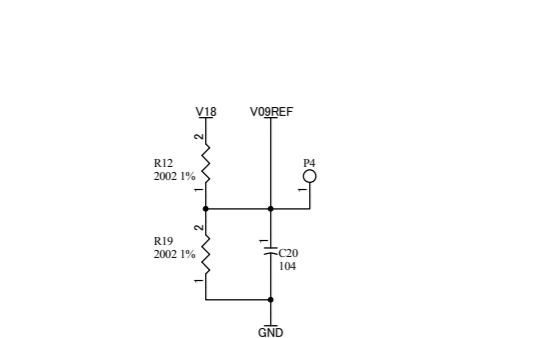
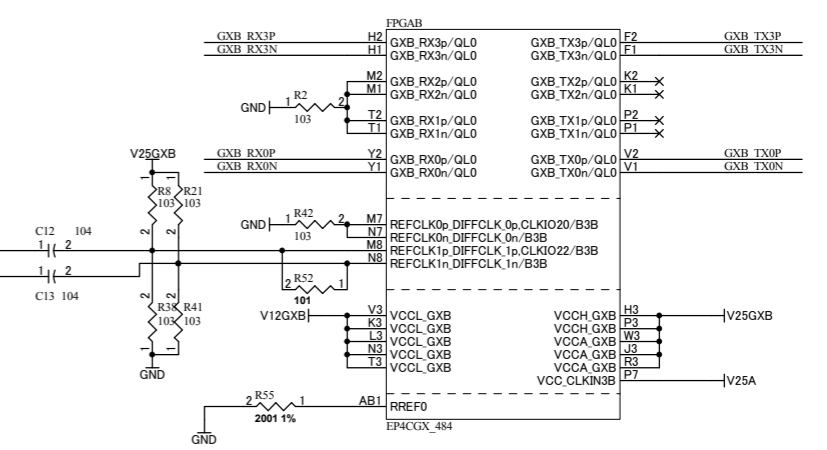
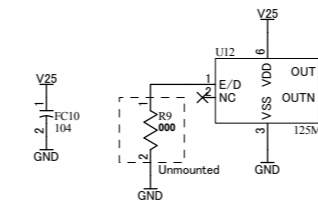
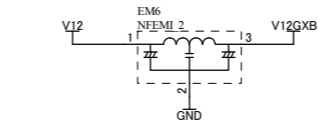
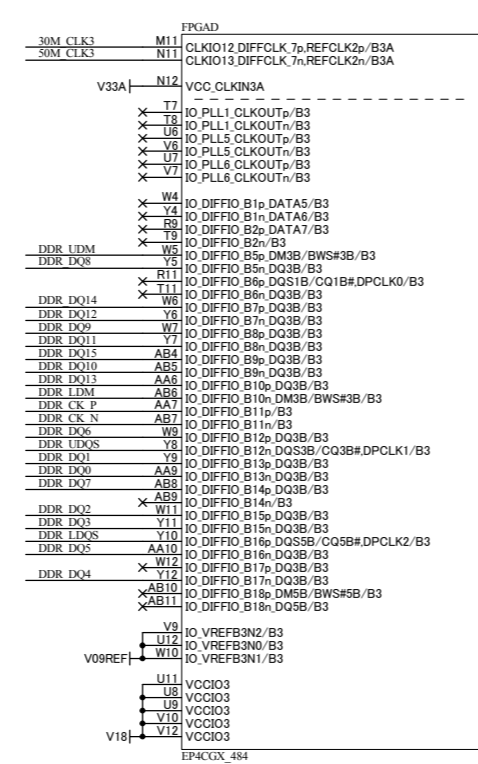
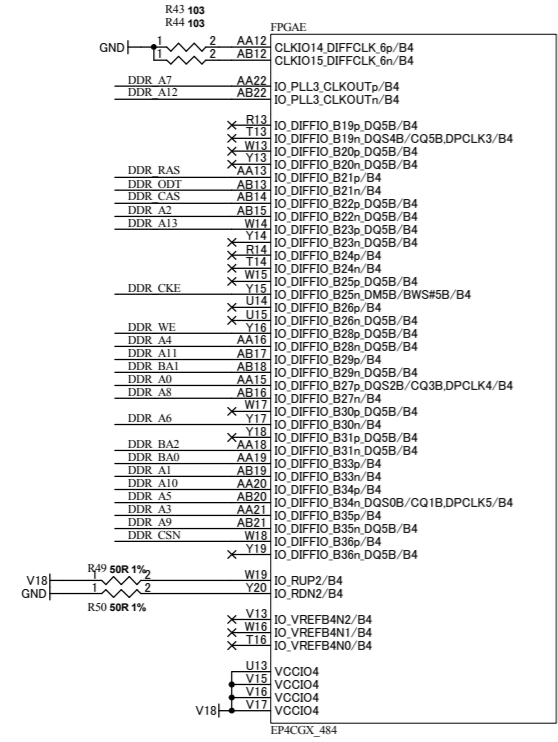
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V33A	V33A
V1Q(B)	V1Q(B)
V25	V25
V25A	V25A
V25GXB	V25GXB
V12	V12
V12D	V12D
V12GXB	V12GXB
V18	V18
V09REF	V09REF
VSB1	VSB1
VSB2	VSB2
GND	GND

30M CLK3	30M CLK3
50M CLK3	50M CLK3
GXB TX3P	GXB TX3P
GXB TX3N	GXB TX3N
GXB RX3P	GXB RX3P
GXB RX3N	GXB RX3N
GXB TX0P	GXB TX0P
GXB TX0N	GXB TX0N
GXB RX0P	GXB RX0P
GXB RX0N	GXB RX0N



LEFT EDGE for HI-SPEED TRASCEIVER

BOTTOM EDGE (BANK 3/4) for DDR2 SDRAM

		ALTERA Cyclone IV GX F484 FPGA board	
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