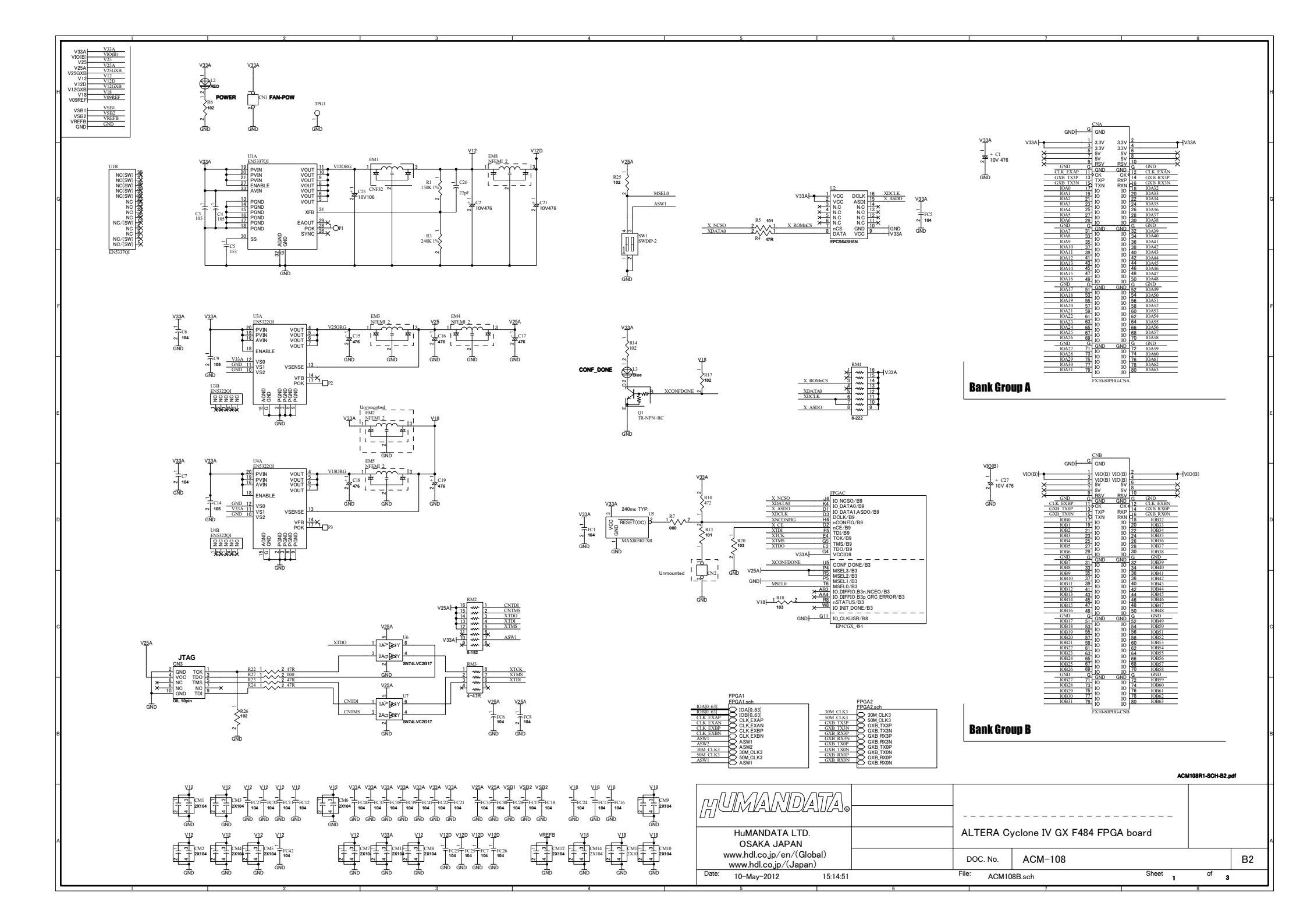
V33A
VIO(B)
V25
V25A
V25GXB
V12
V12D
V12GXB
V18
V09REF
VSB1
VSB2
VREFB
GND
POWER
FAN-POW
TPG1
U1A
EN5337QI
U1B
V12ORG
U3A
EN5322QI
V25ORG
U4A
V18ORG
U3B
U4B
Unmounted
CONF_DONE
Q1
TR-NPN+RC
XCONFDONE
X_NCSO
XDATA0
X_ROMnCS
XDCLK
X_ASDO
EPCS64SI16N
FPGAC
IO_NCSO/B9
IO_DATA0/B9
IO_DATA1/ASDO/B9
DCLK/B9
nCONFIG/B9
nCE/B9
TDI/B9
TCK/B9
TMS/B9
TDO/B9
VCCIO9
CONF_DONE/B3
MSEL3/B3
MSEL2/B3
MSEL1/B3
MSEL0/B3
IO_DIFFIO_B3n,NCEO/B3
IO_DIFFIO_B3p,CRC_ERROR/B3
nSTATUS/B3
IO_INIT_DONE/B3
IO_CLKUSR/B8
EP4CGX_484
240ms TYP.
MAX803REXR
JTAG
DIL 10pin
SN74LVC2G17
8-152
4-47R
8-222
CNA
CNB
FX10-80PHG-CNA
FX10-80PHG-CNB
Bank Group A
Bank Group B
FPGA1
FPGA1.sch
FPGA2
FPGA2.sch
ACM108R1-SCH-B2.pdf
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10−May−2012
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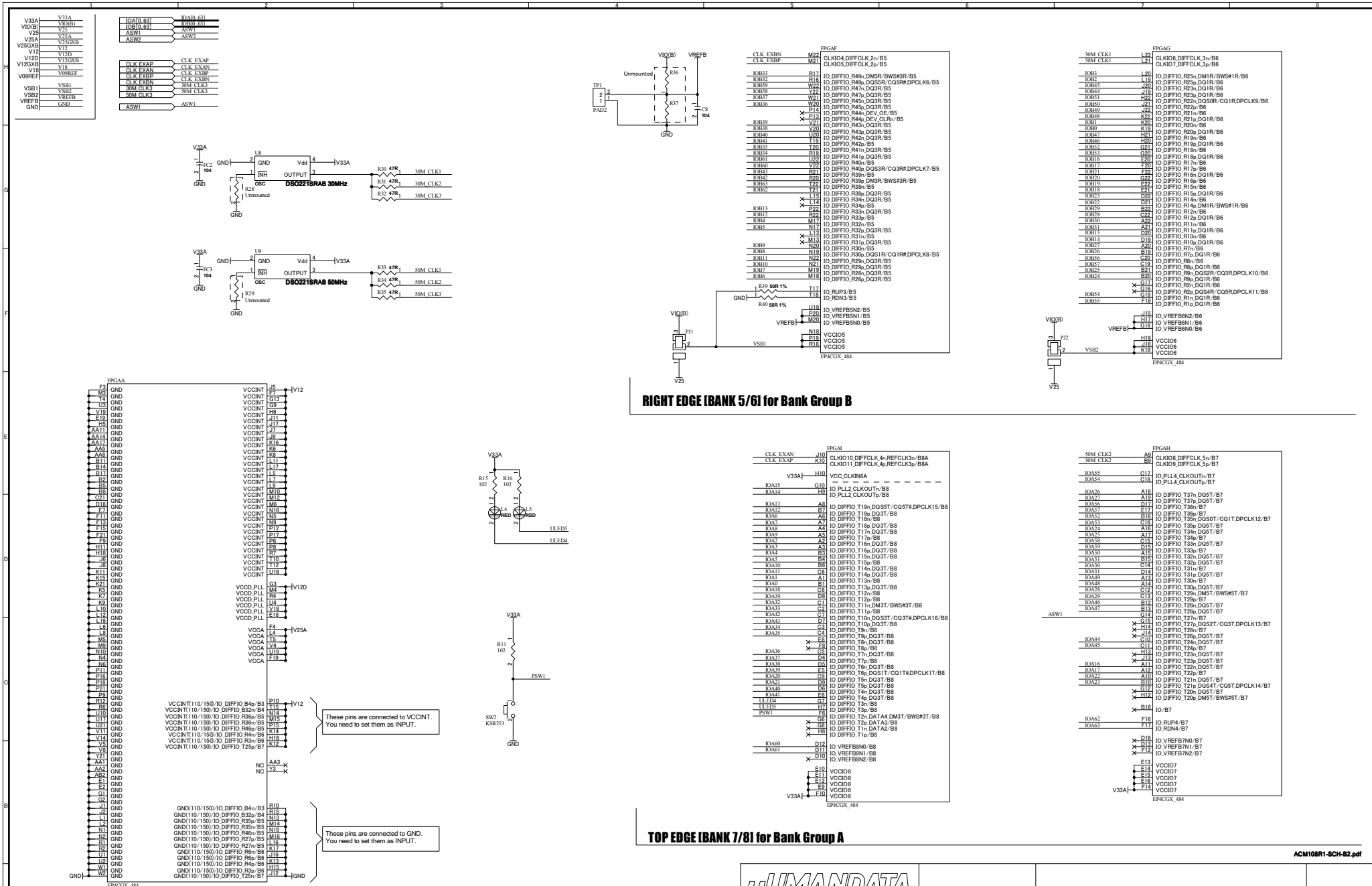

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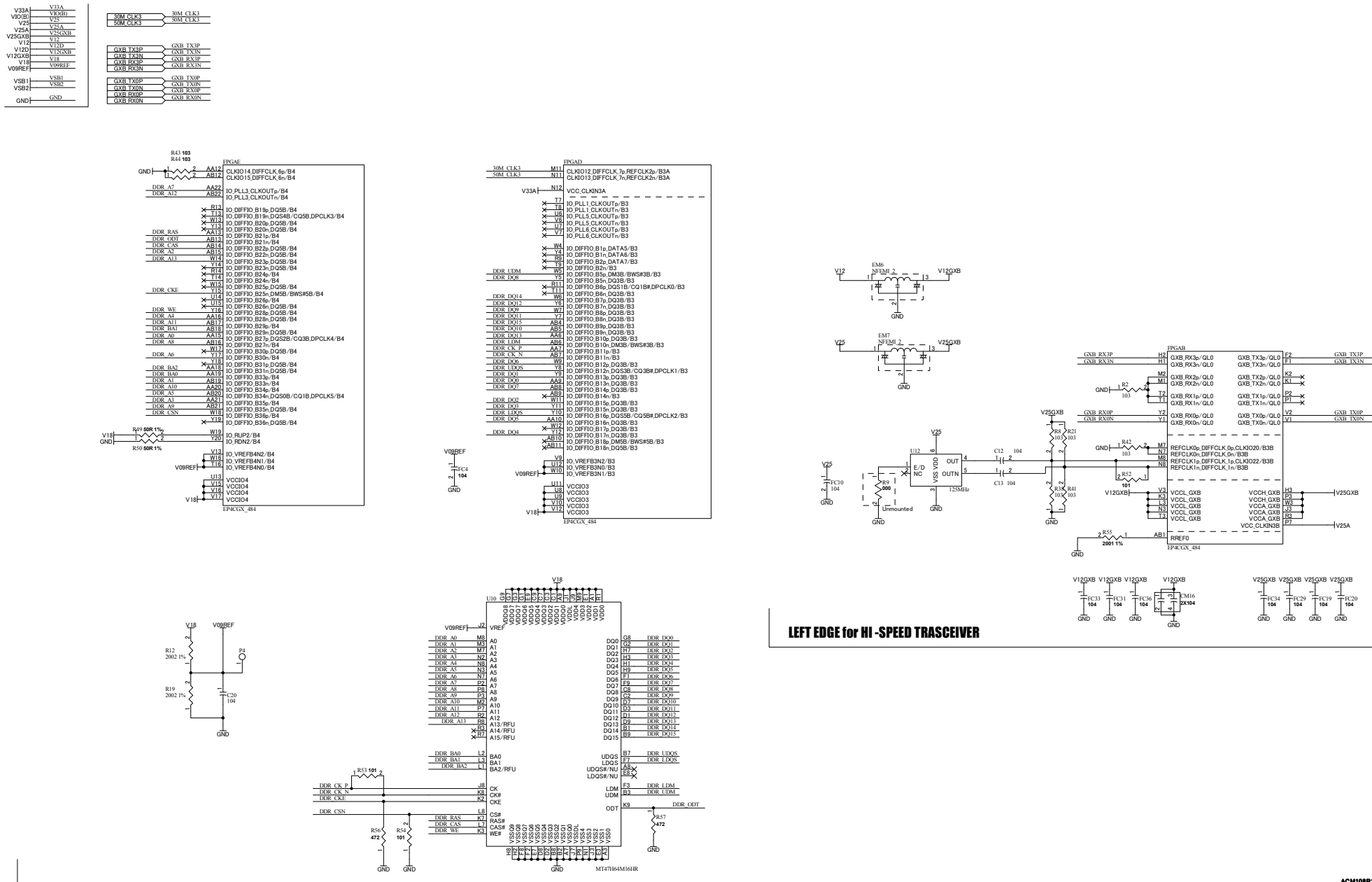

LEFT EDGE for HI -SPEED TRASCEIVER

BOTTOM EDGE [BANK 3/4] for DDR2 SDRAM

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	DOC. No.	ACM−108 B2
Date: 10−May−2012 15:14:52	File: FPGA2.sch	Sheet 3 of 3