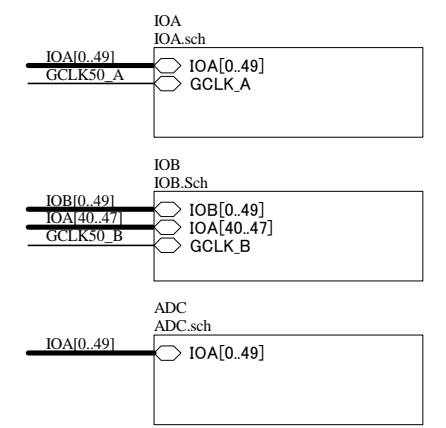


CNA	VIO(A)	VIO(B)
1	VIO(A)	VIO(B)
2	VIO(A)	VIO(B)
3	5V	5V
4	5V	5V
5	GND	GND
6	GND	GND
7	IOA0	IOB0
8	IOA1	IOB1
9	IOA2	IOB2
10	IOA3	IOB3
11	IOA4	IOB4
12	IOA5	IOB5
13	IOA6	IOB6
14	IOA7	IOB7
15	GND	GND
16	GND	GND
17	IOA8	IOB8
18	IOA9	IOB9
19	IOA10	IOB10
20	IOA11	IOB11
21	IOA12	IOB12
22	IOA13	IOB13
23	IOA14	IOB14
24	IOA15	IOB15
25	GND	GND
26	GND	GND
27	IOA16	IOB16
28	IOA17	IOB17
29	IOA18	IOB18
30	IOA19	IOB19
31	IOA20	IOB20
32	IOA21	IOB21
33	IOA22	IOB22
34	IOA23	IOB23
35	GND	GND
36	GND	GND
37	IOA24	IOB24
38	IOA25	IOB25
39	IOA26	IOB26
40	IOA27	IOB27
41	IOA28	IOB28
42	IOA29	IOB29
43	IOA30	IOB30
44	IOA31	IOB31
45	GND	GND
46	GND	GND
47	IOA32	IOB32
48	IOA33	IOB33
49	IOA34	IOB34
50	IOA35	IOB35
51	IOA36	IOB36
52	IOA37	IOB37
53	IOA38	IOB38
54	IOA39	IOB39
55	GND	GND
56	GND	GND
57	IOA40	IOB40
58	IOA41	IOB41
59	IOA42	IOB42
60	IOA43	IOB43
61	IOA44	IOB44
62	IOA45	IOB45
63	IOA46	IOB46
64	IOA47	IOB47
65	IOA48	IOB48
66	IOA49	IOB49

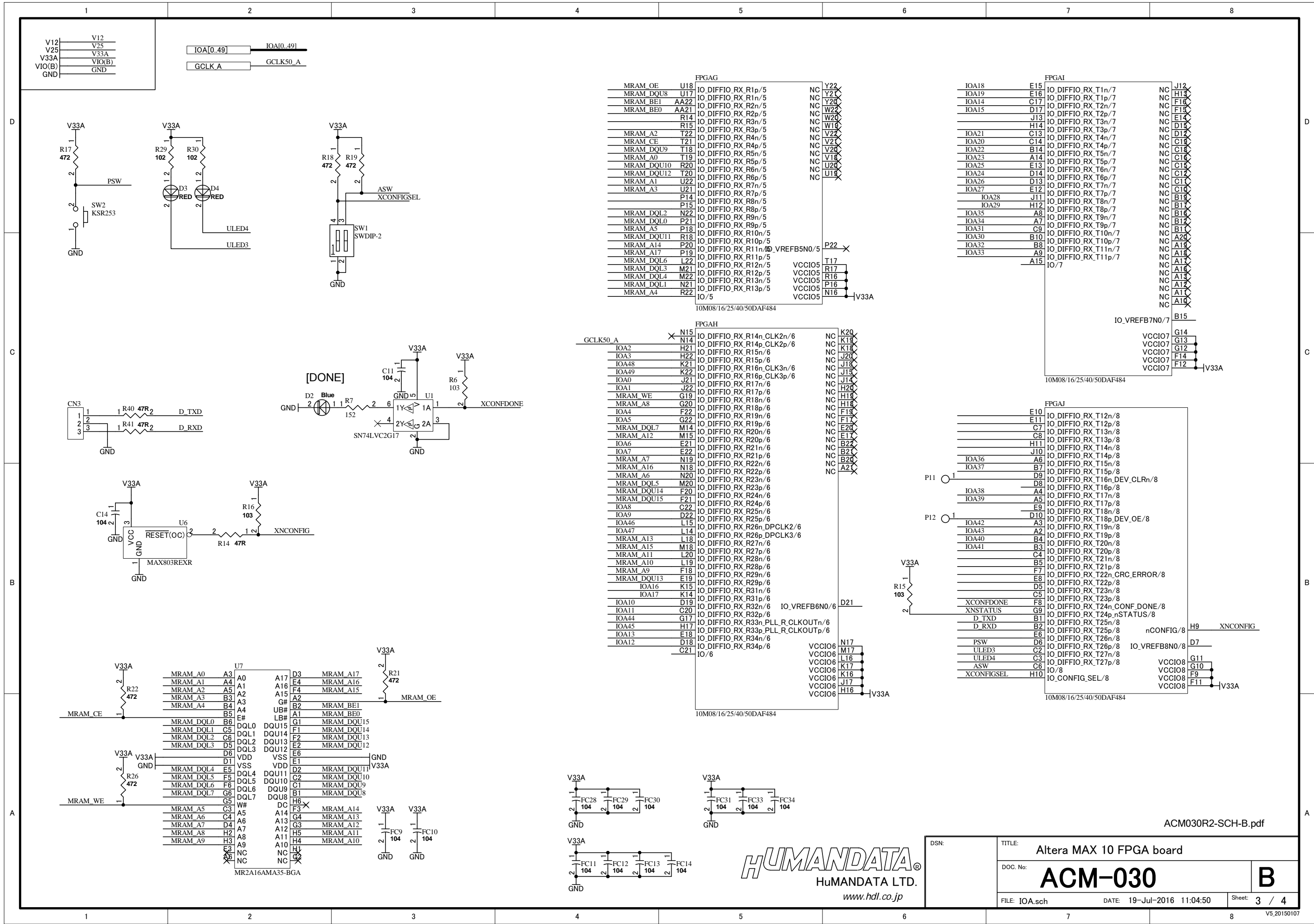


IOA40 to IOA47 are
parallely connected to ADC Pins



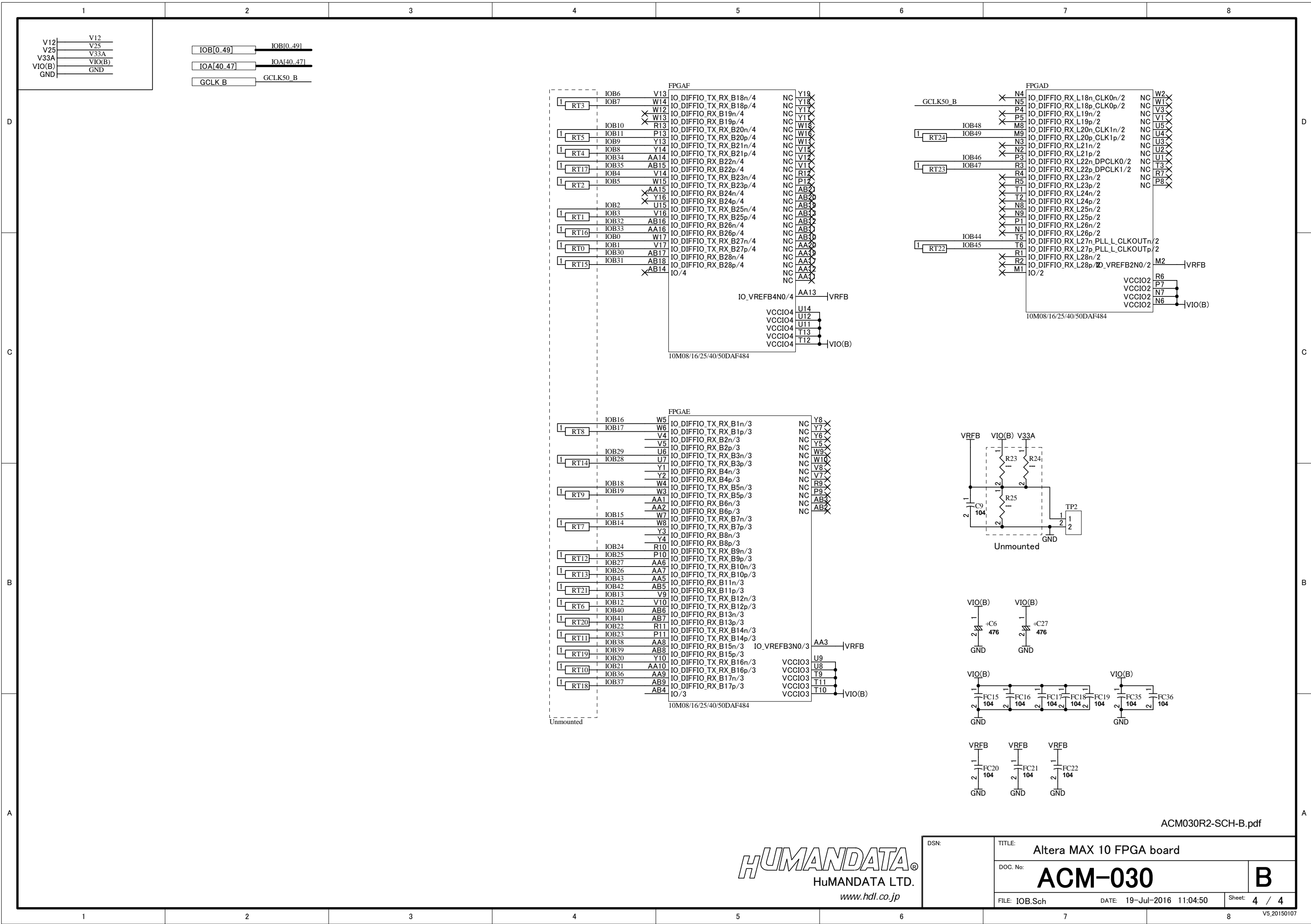
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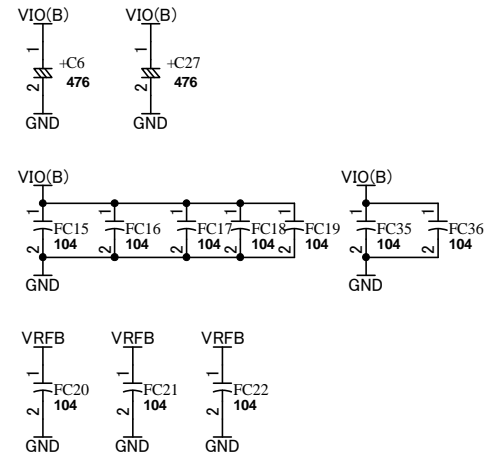
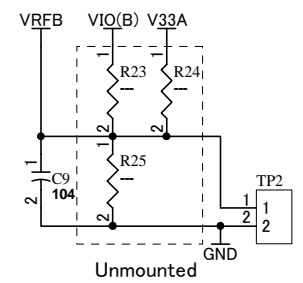
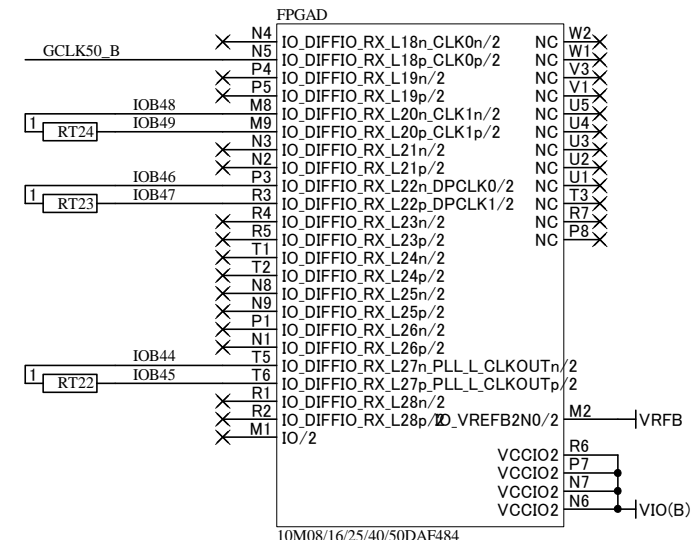
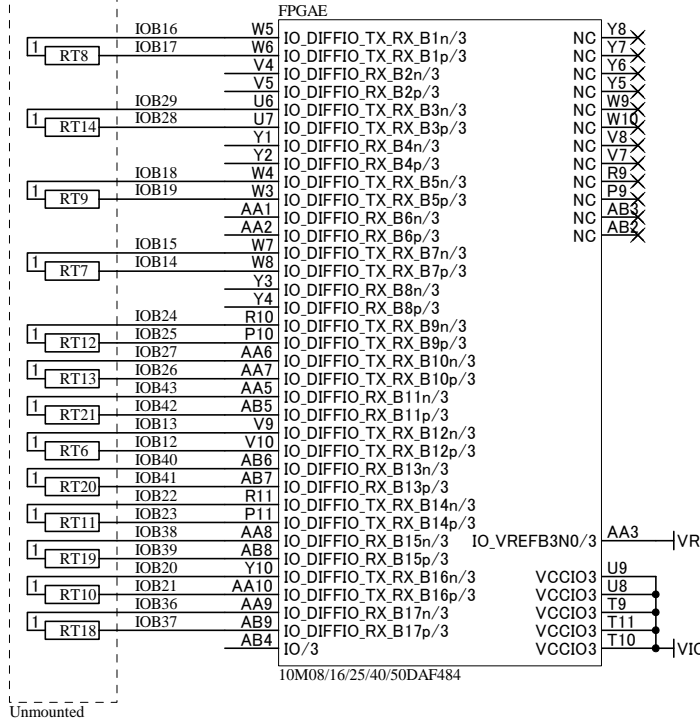
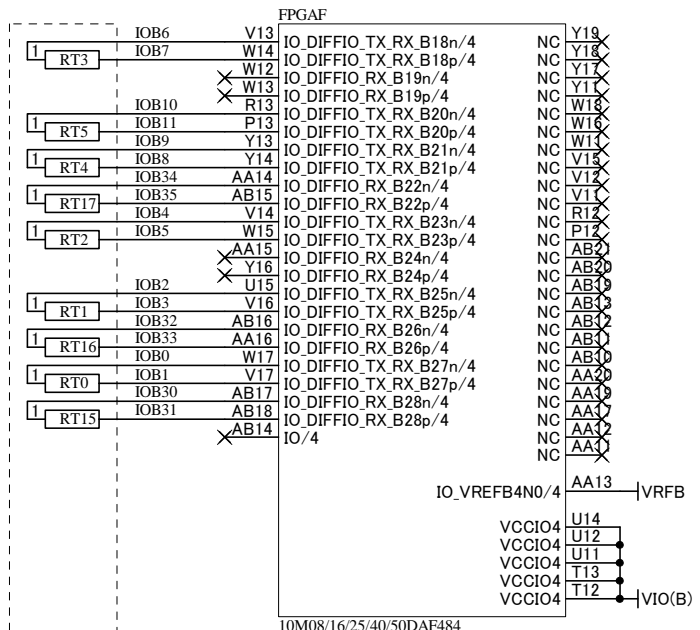
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Sheet: 3 / 4	V5.20150107

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V12 V12
 V25 V25
 V33A V33A
 VIO(B) VIO(B)
 GND GND

IOB[0..49] IOB[0..49]
 IOA[40..47] IOA[40..47]
 GCLK_B GCLK50_B



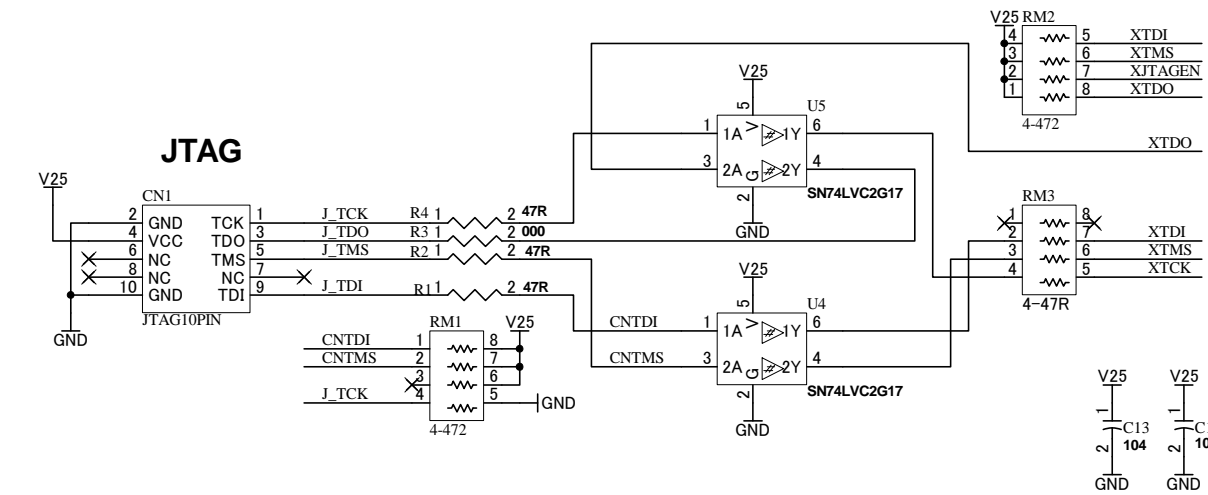
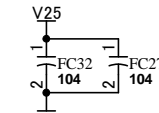
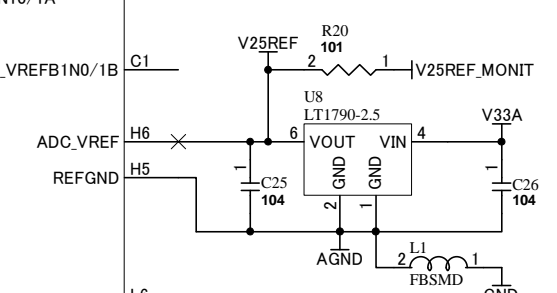
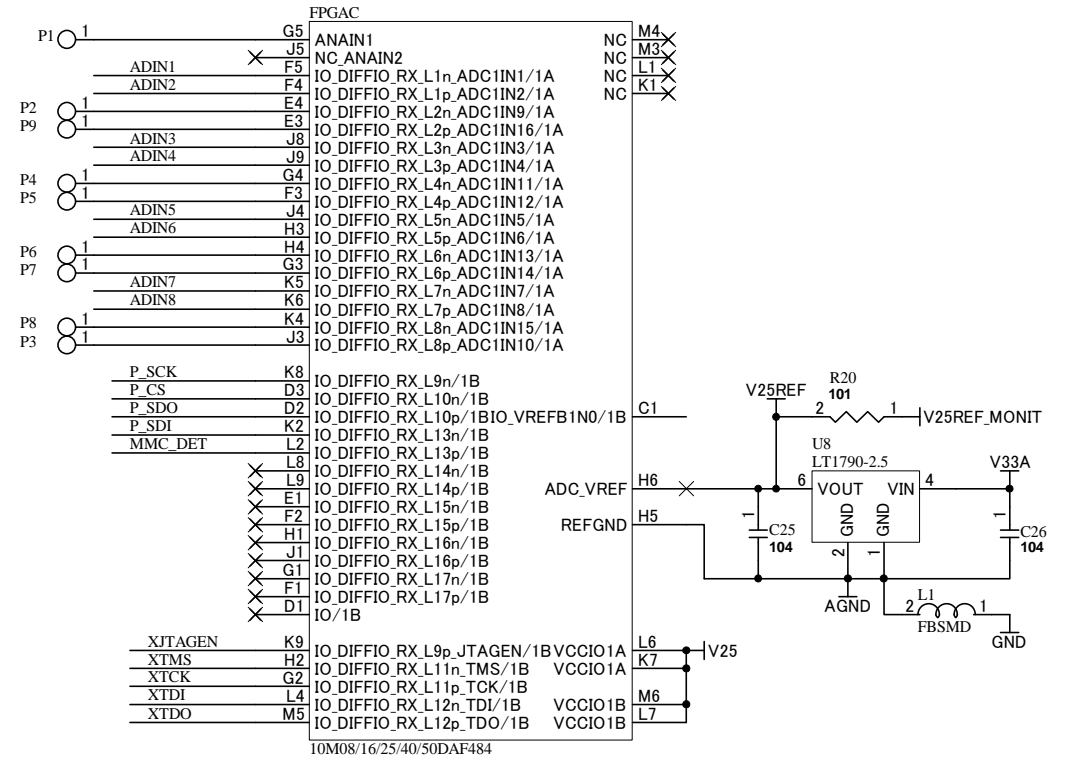
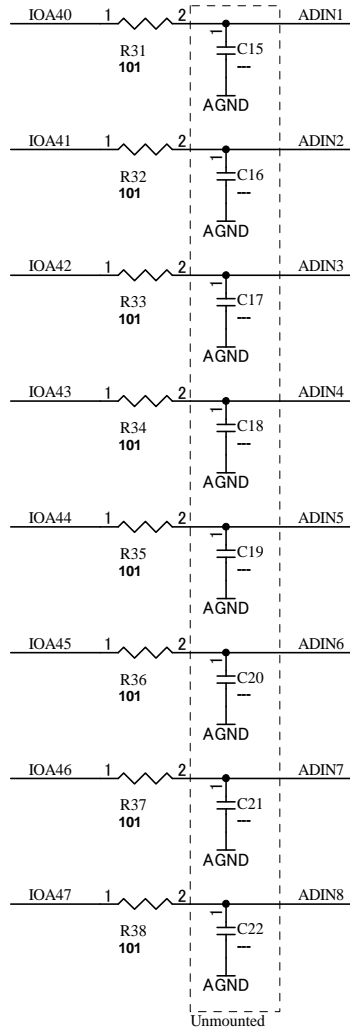
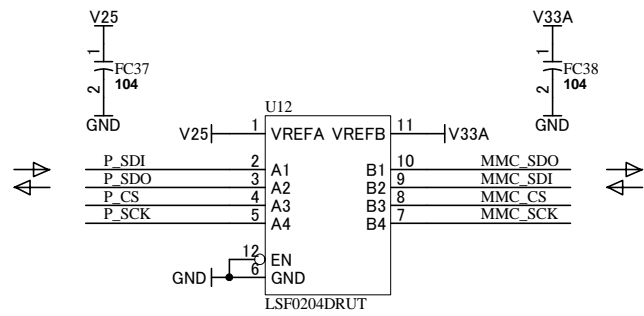
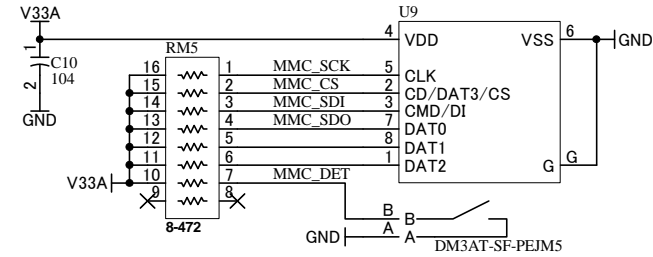
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Sheet: 4 / 4	V5.20150107

V12
V25
V33A
VIO(B)
GND

IOA[0..49] IOA[0..49]



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DSN:	TITLE: Altera MAX 10 FPGA board
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