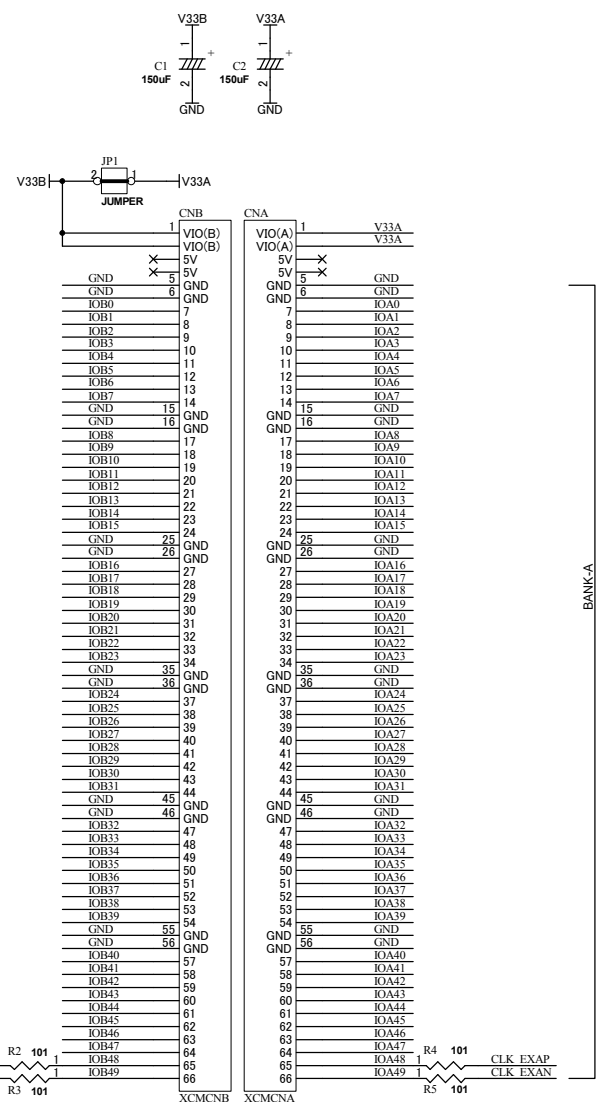
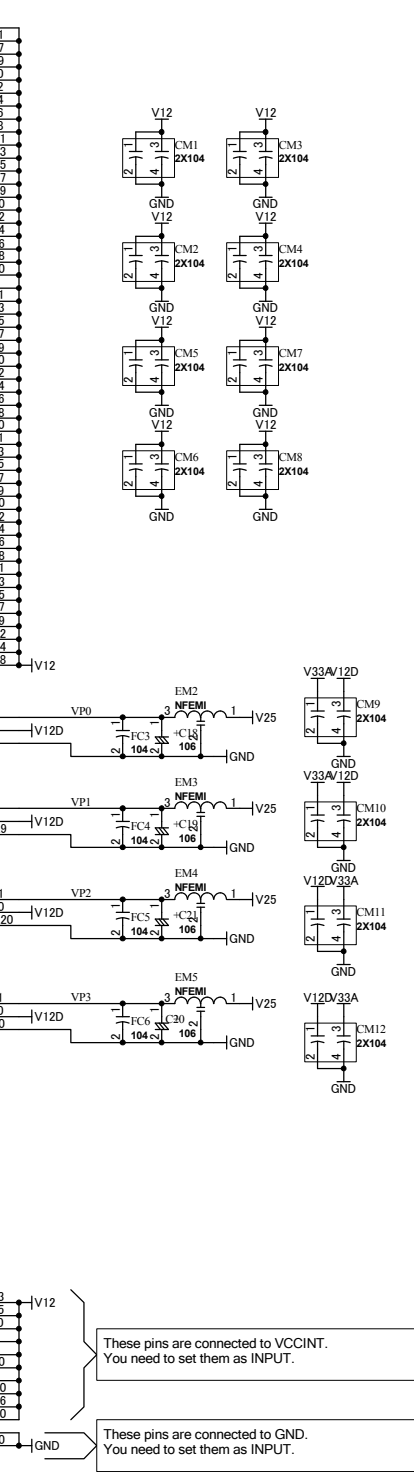
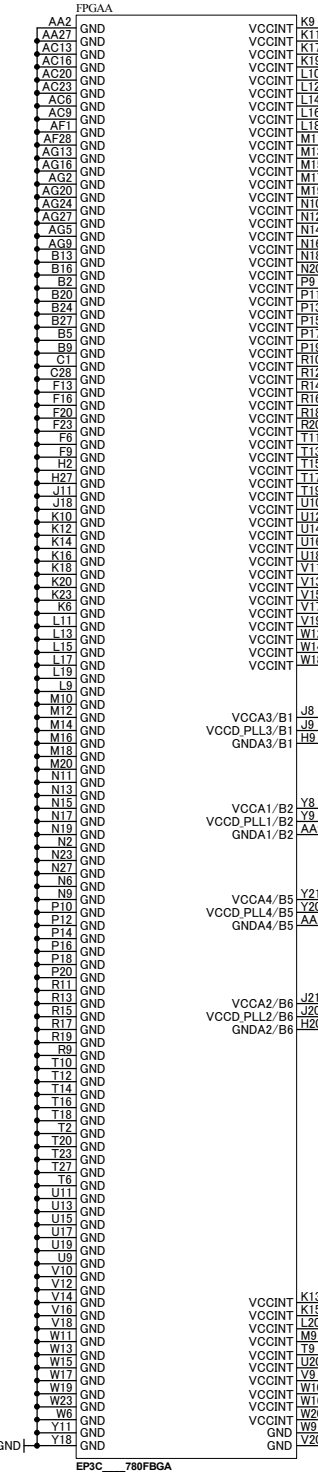


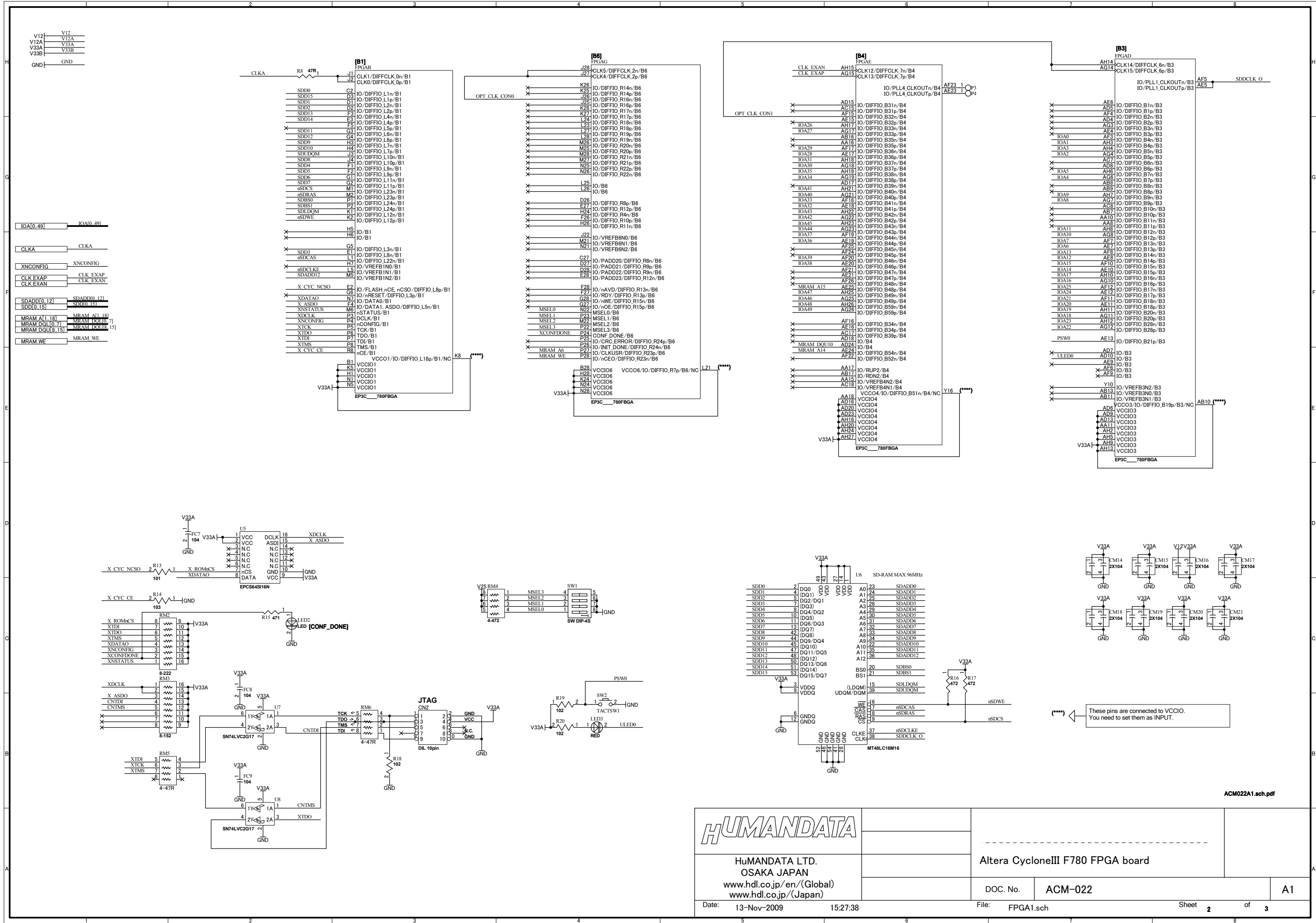
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CLKA	CLKA
XNCONFIG	XNCONFIG
CLK_EXAP	CLK_EXAP
CLK_EXAN	CLK_EXAN
SDADD[0..12]	SDADD[0..12]
SDADD[13]	SDADD[13]
SDADD[14]	SDADD[14]
MRAM_A[1..18]	MRAM_A[1..18]
MRAM_DQ[0..7]	MRAM_DQ[0..7]
MRAM_DQ[8..15]	MRAM_DQ[8..15]
MRAM_WE	MRAM_WE


IOB[0..49]	IOB[0..49]
CLK_EXBP	CLK_EXBP
CLK_EXBN	CLK_EXBN
SDADD[0..12]	SDADD[0..12]
SDADD[13]	SDADD[13]
SDADD[14]	SDADD[14]
MRAM_A[1..18]	MRAM_A[1..18]
MRAM_DQ[0..7]	MRAM_DQ[0..7]
MRAM_DQ[8..15]	MRAM_DQ[8..15]
MRAM_WE	MRAM_WE



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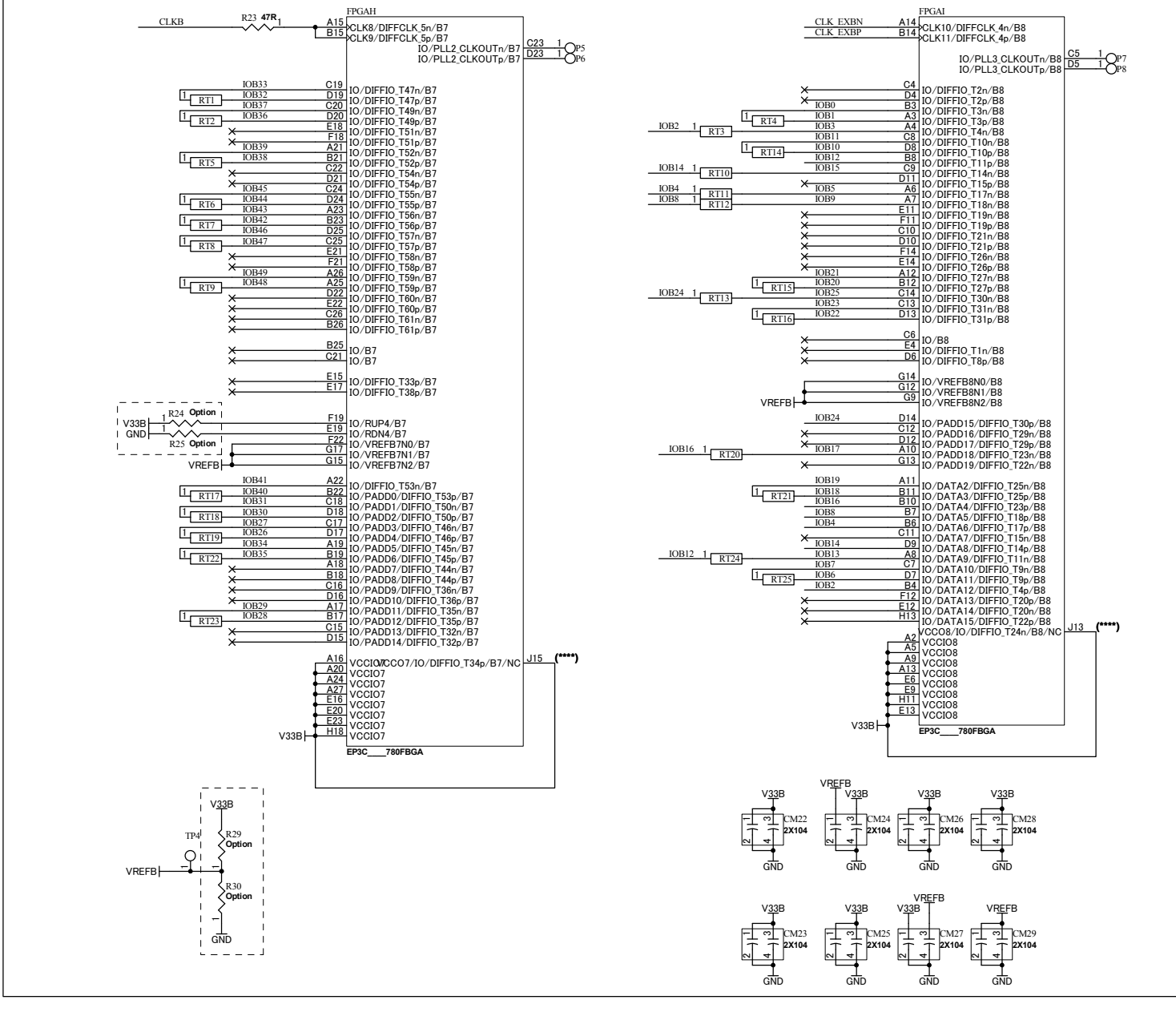
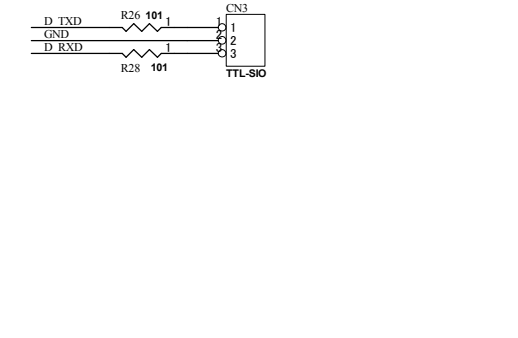
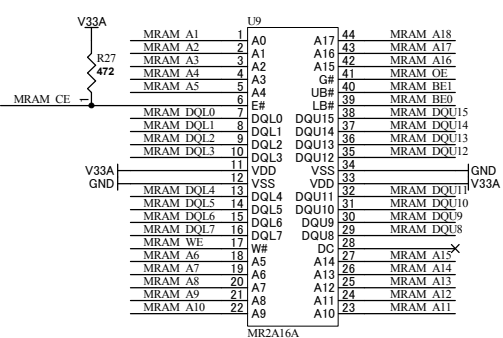
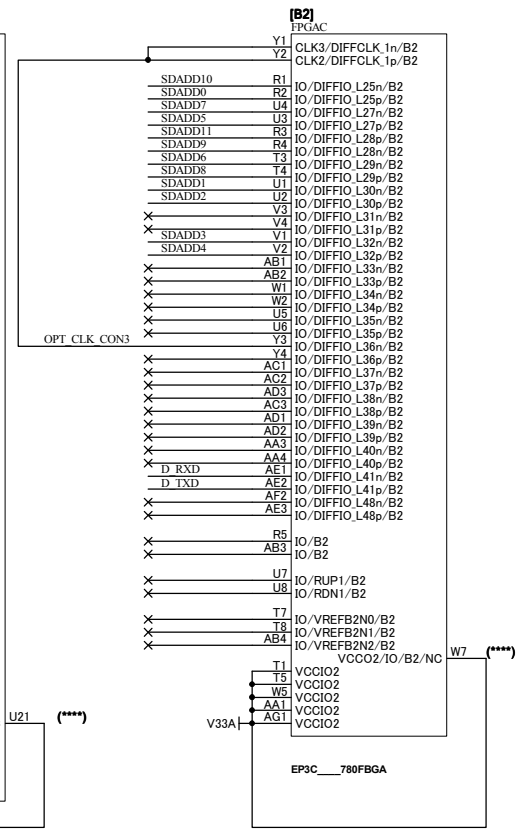
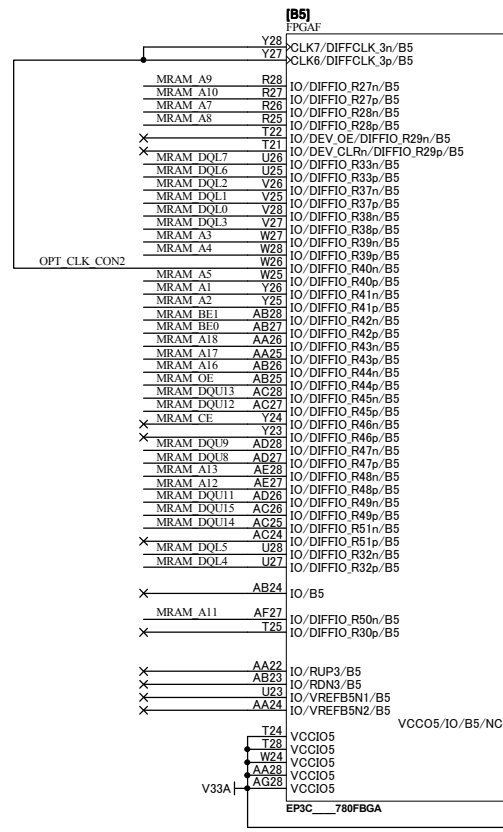
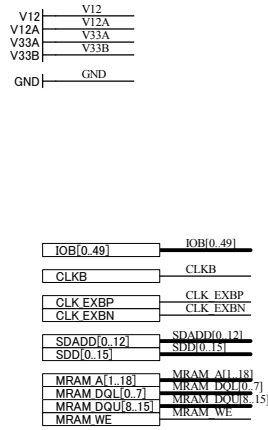


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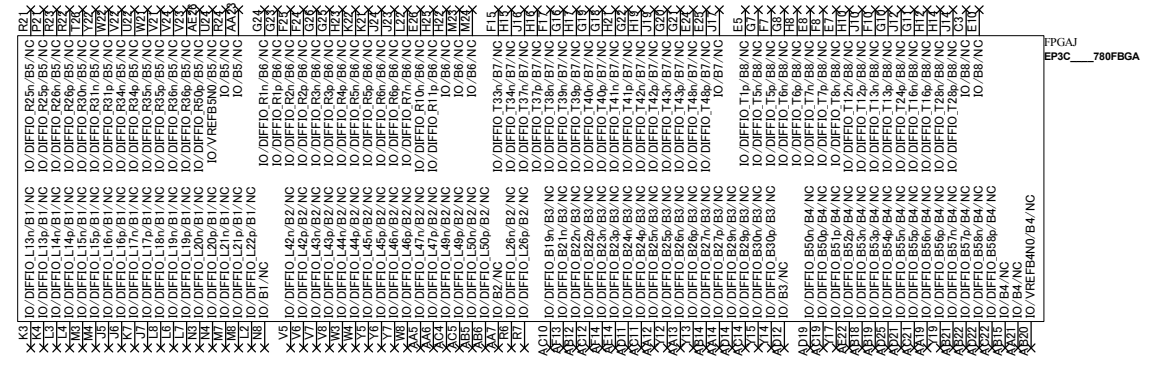
Altera CycloneIII F780 FPGA board

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(****) These pins are connected to VCCIO. You need to set them as INPUT.



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