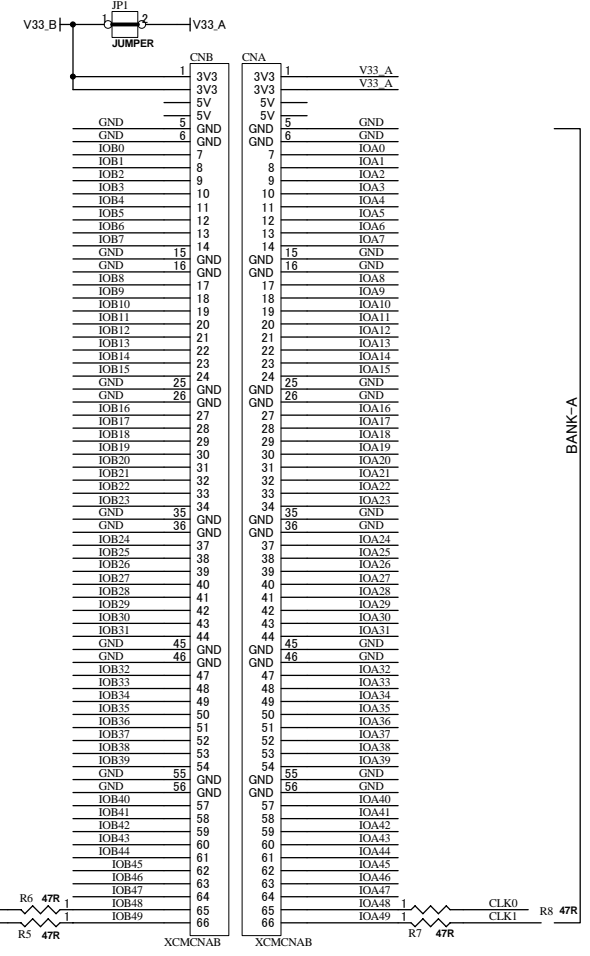
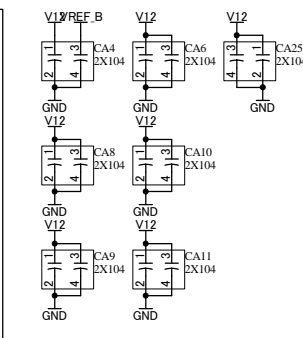
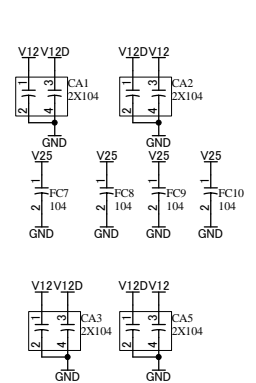
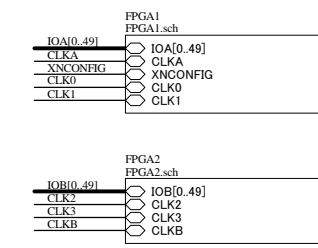
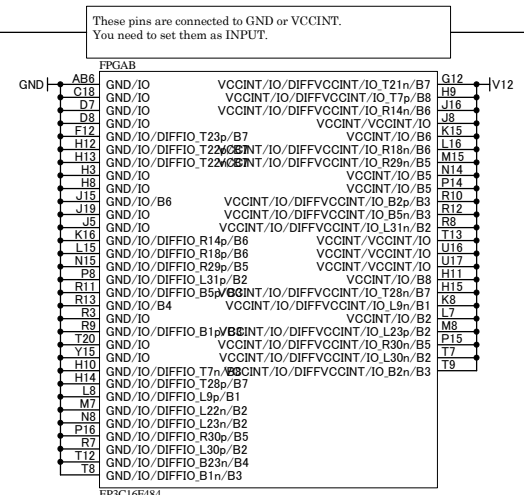
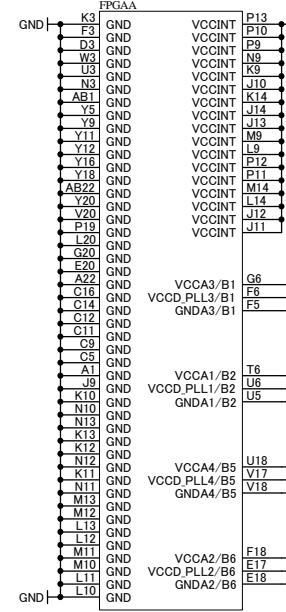
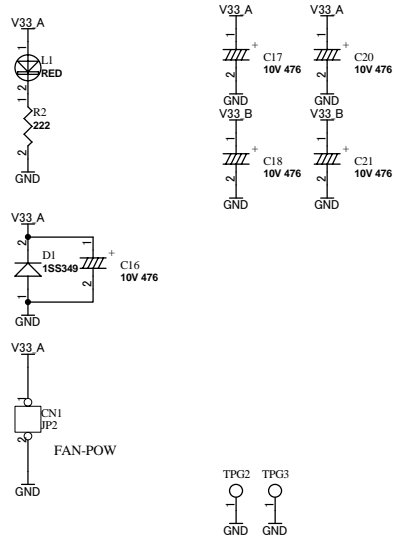
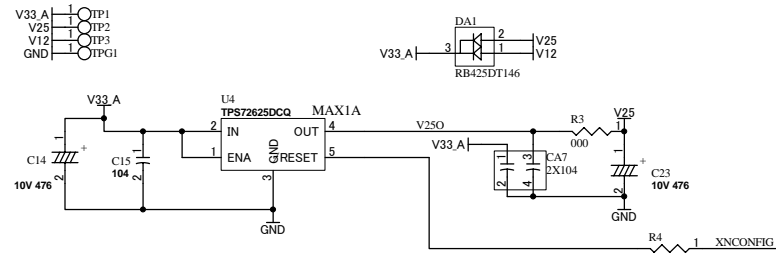
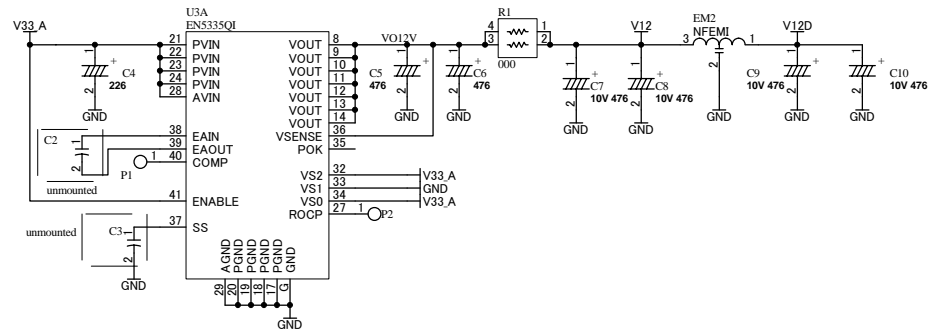
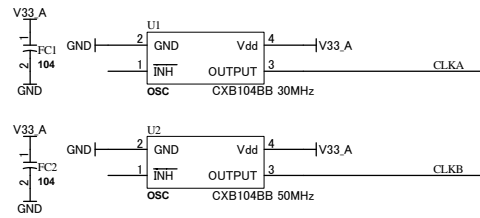


V12 V12  
 V25 V25  
 V33\_A V33\_A  
 V33\_B V33\_B  
 V33C V33C  
 GND GND



**HUMAN DATA**

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Cyclone3 Bread Board( F484 )

DOC. No. ACM-021

Date: 14-Sep-2009 10:17:15

File: ACM021A.sch

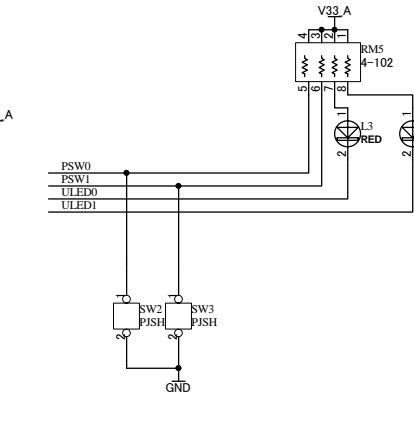
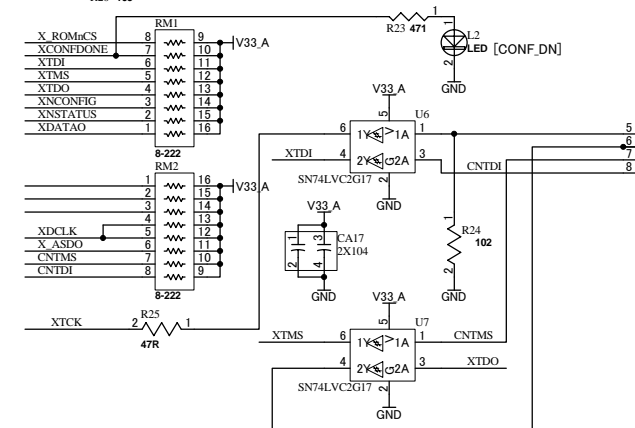
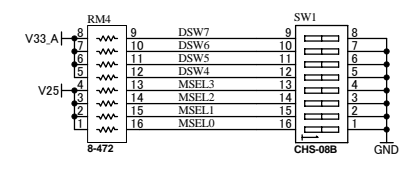
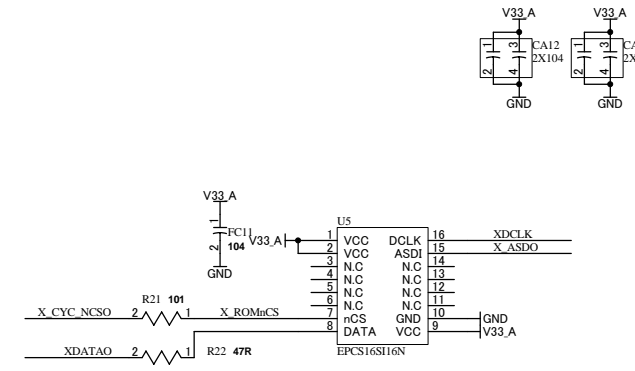
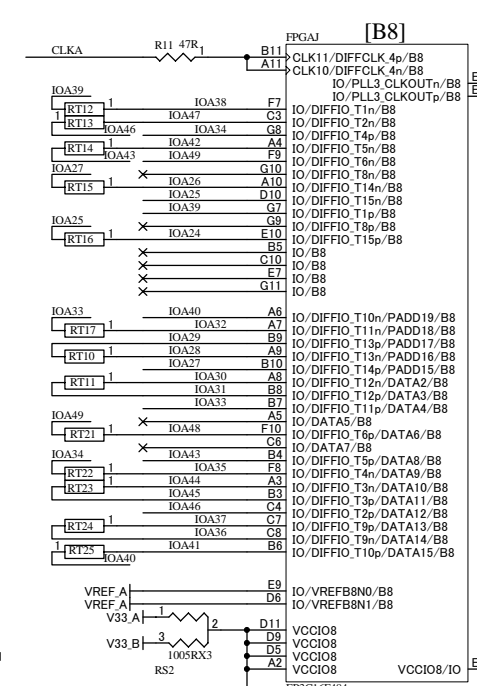
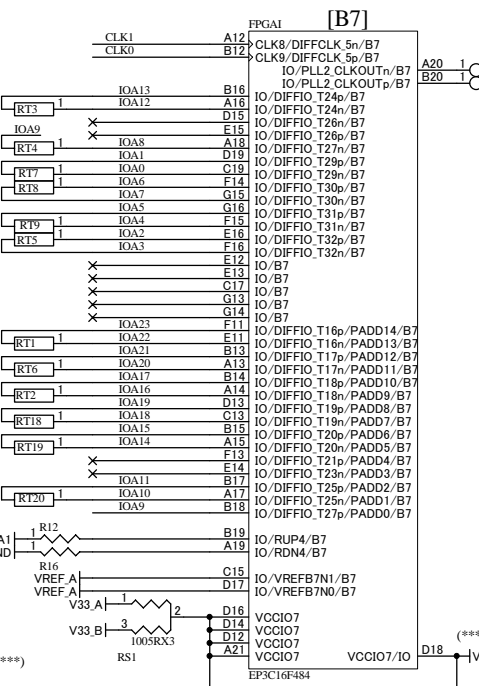
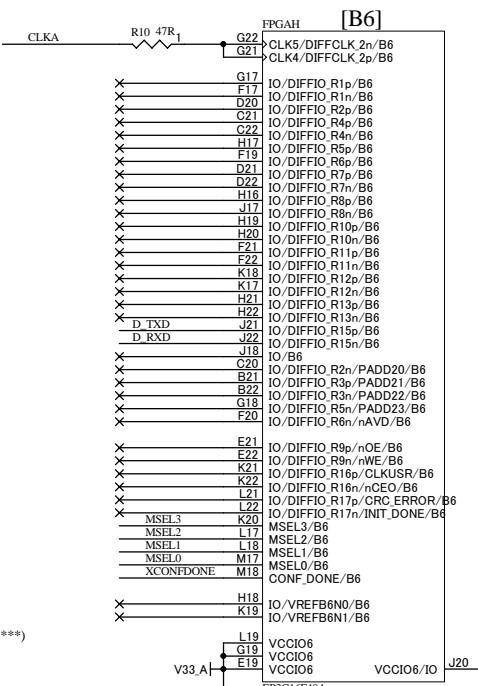
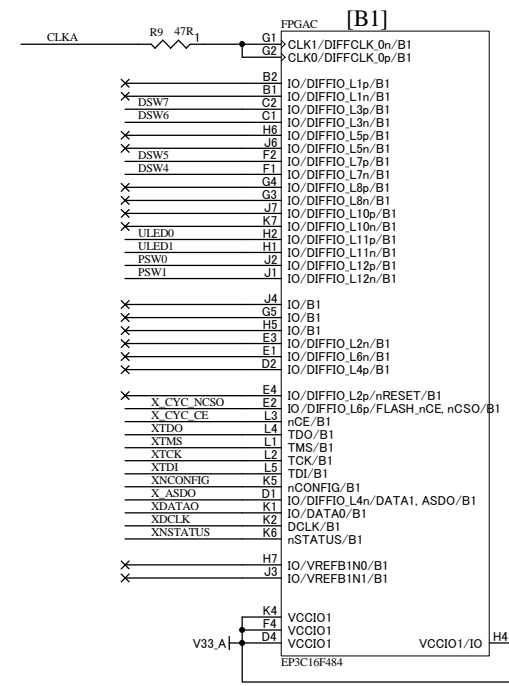
Sheet 1 of 3

A1

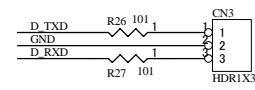
V12 V12A  
 V33 A V33\_A  
 V33 B V33\_B  
 V33C V33C

GND GND

IOA[0..49] IOA[0..49]  
 CLKA CLKA  
 XNCONFIG XNCONFIG  
 CLK0 CLK0  
 CLK1 CLK1



(\*\*\*\*) These pins are connected to GND or VCCINT. You need to set them as INPUT.



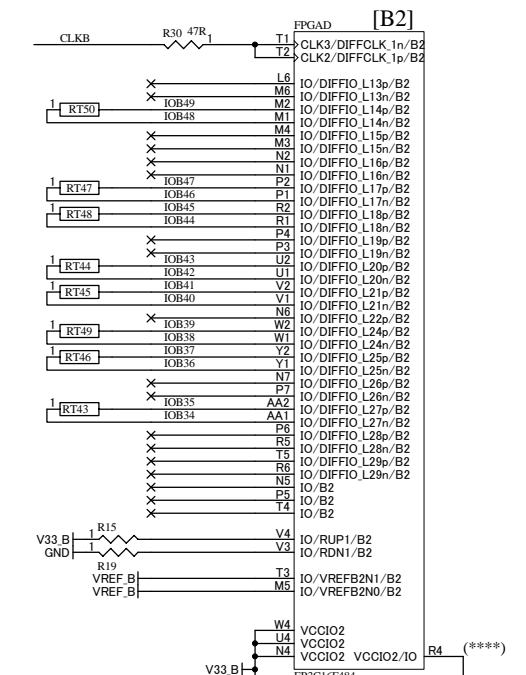
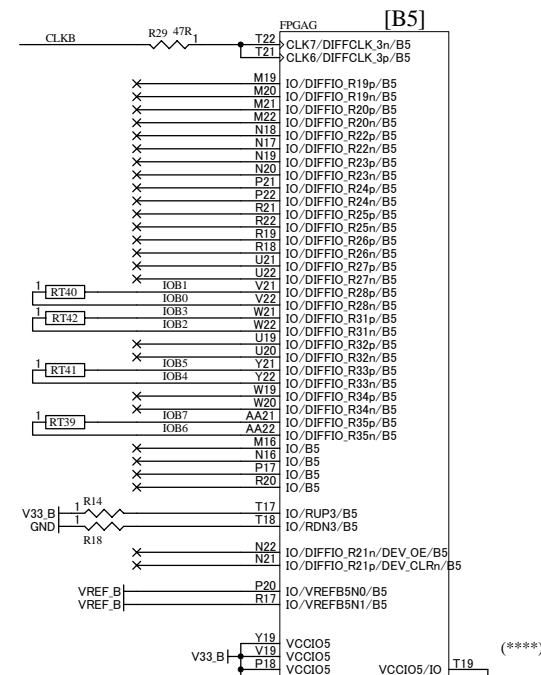
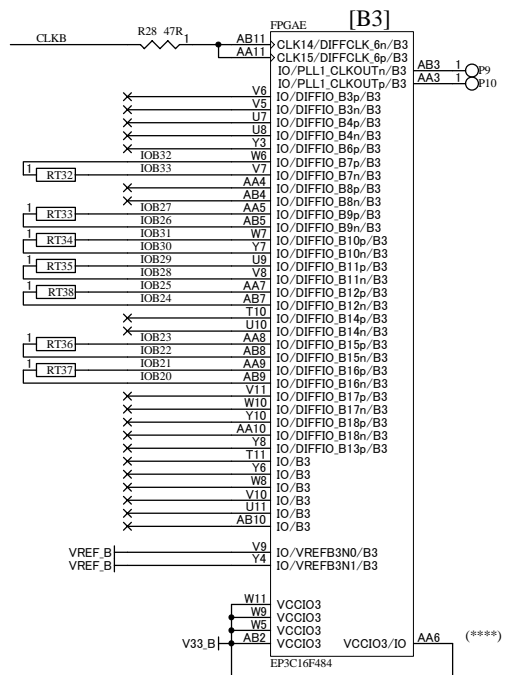
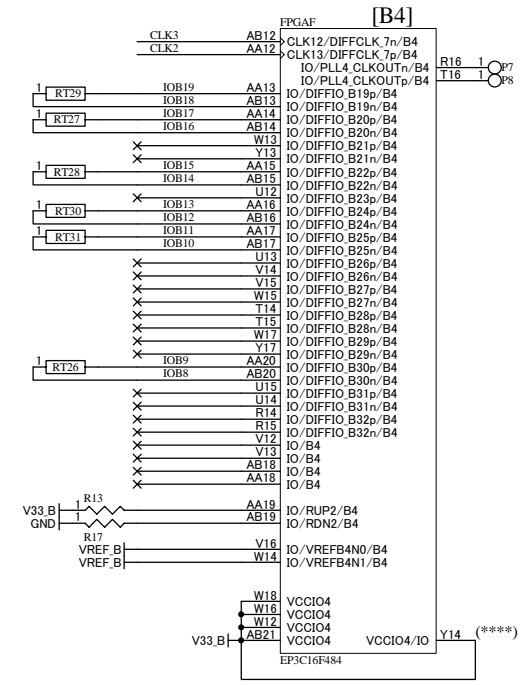
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Date: 14-Sep-2009	10:16:02	DOC. No. ACM-021	A1
File: FPGA1.sch		Sheet 2	of 3

V12 V12  
V12A V12A  
V33 A V33 A  
V33 B V33 B

GND GND

IOB(0..49) IOB(0..49)  
CLKB CLKB

CLK2 CLK2  
CLK3 CLK3



[B2]

(\*\*\*\*) These pins are connected to GND or VCCINT. You need to set them as INPUT.

<b>HUMAN DATA</b>			
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Date: 14-Sep-2009	10:17:31	DOC. No. ACM-021	A1
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