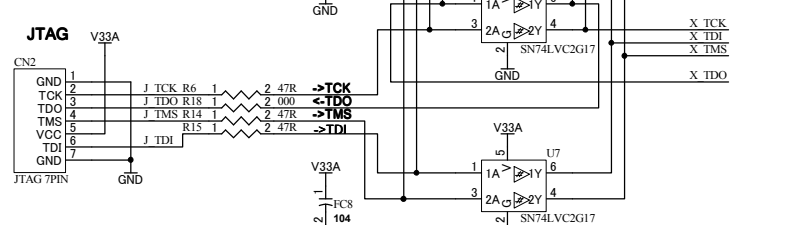
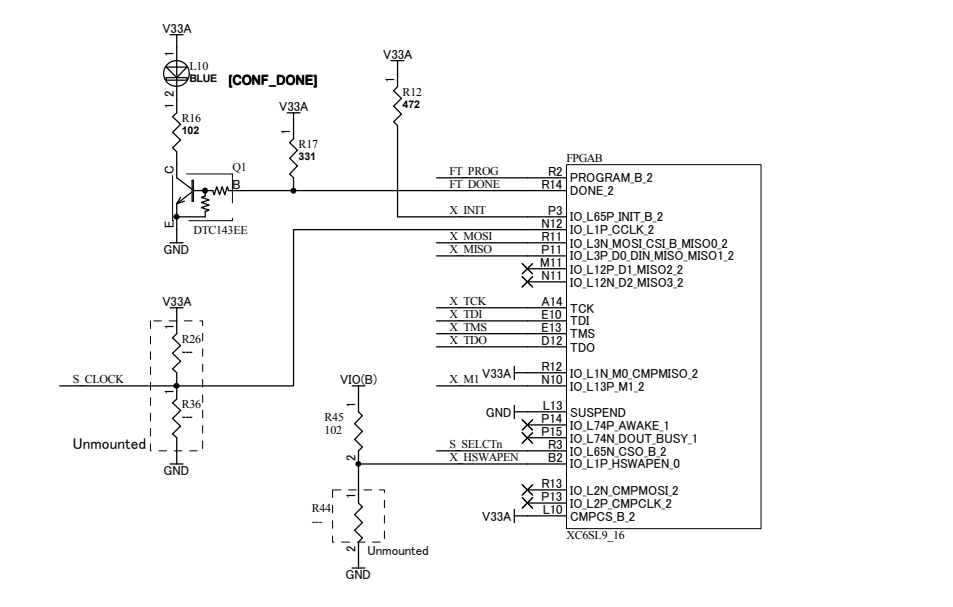
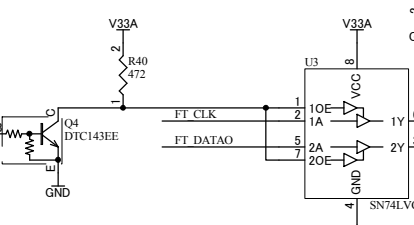
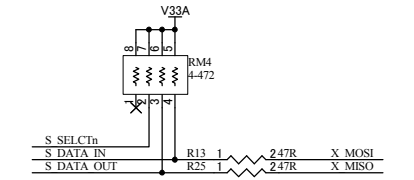
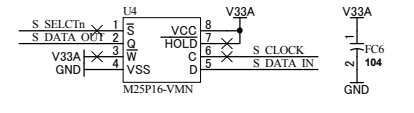
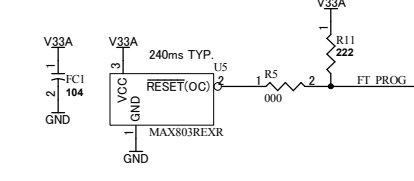
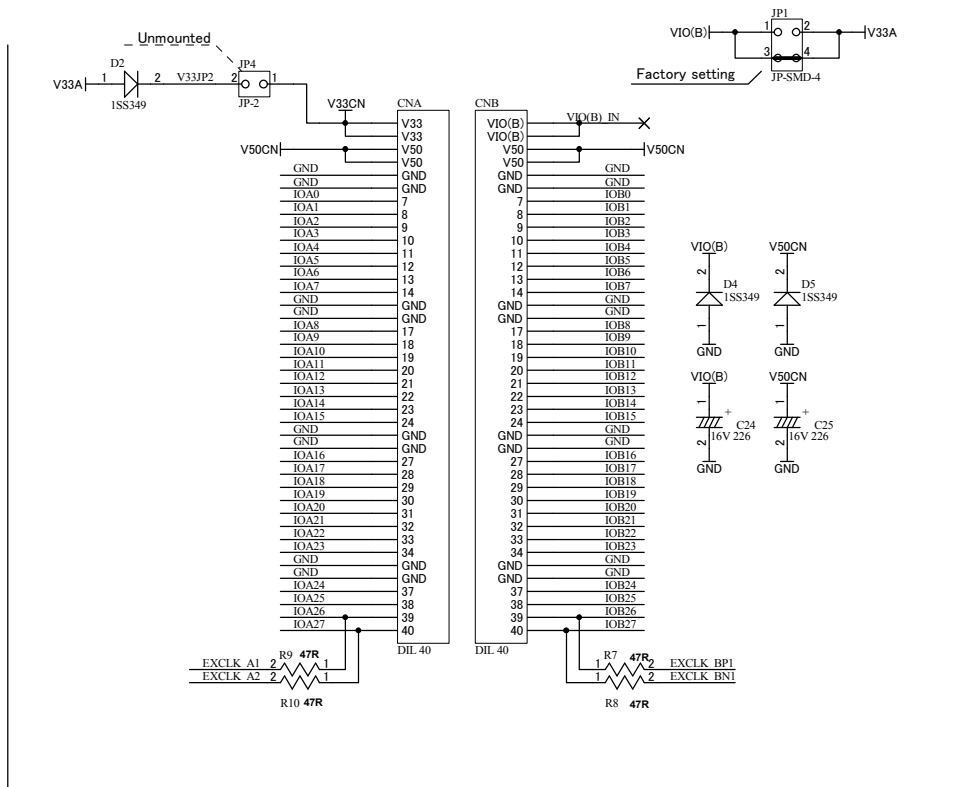


V50CN	V50CN
V33CN	V33CN
V50USB	V50USB
V50ORG	V50ORG
V33A	V33A
V12D	V12D
V12	V12
GND	GND

FPGA	
A1	GND
B10	GND
B8	GND
C13	GND
C3	GND
E11	GND
F14	GND
F2	GND
F6	GND
G7	GND
G9	GND
H8	GND
H7	GND
J7	GND
J9	GND
K14	GND
K2	GND
K6	GND
L11	GND
N13	GND
N3	GND
P10	GND
P6	GND
R1	GND
R15	GND
GND	GND
FPGA	
F9	VCCINT
G6	VCCINT
H6	VCCINT
H9	VCCINT
J10	VCCINT
J8	VCCINT
K7	VCCINT
FPGA	
B1	VCCAUX
F7	VCCAUX
G10	VCCAUX
J6	VCCAUX
K9	VCCAUX
L4	VCCAUX
M12	VCCAUX
FPGA	
XC6SL9_16	



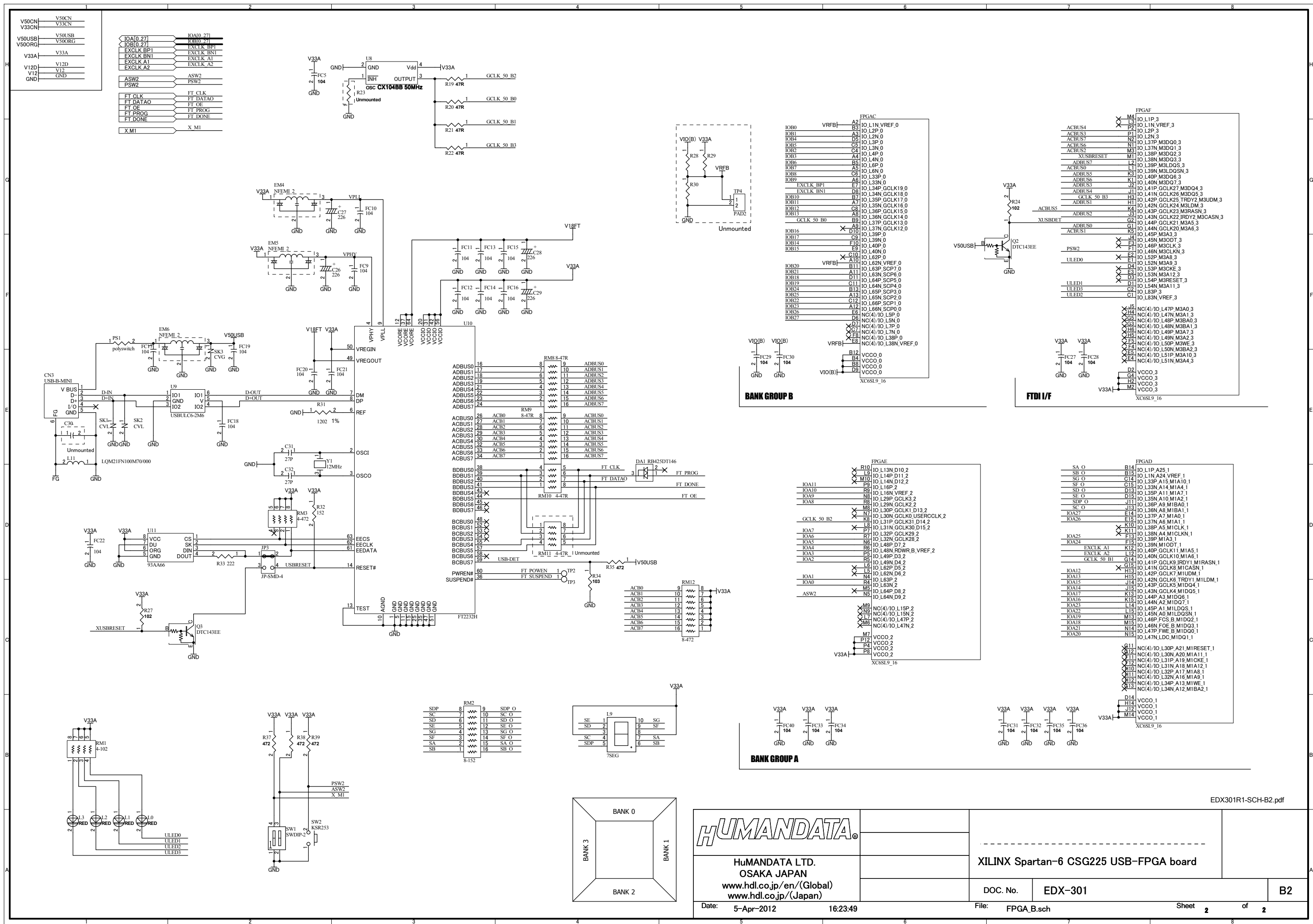
V33A	V33A	V33A	V12	V12	V12	V12	V33A	V33A	V33A	V33A
FC37	FC38	FC39	FC2	FC2	FC25	FC26	FC3	FC4	FC41	FC42
104	104	104	104	104	104	104	104	104	104	104
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

IOA[0..27]	IOA[0..27]
IOB[0..27]	IOB[0..27]
EXCLK_BP1	EXCLK_BP1
EXCLK_BN1	EXCLK_BN1
EXCLK_A1	EXCLK_A1
EXCLK_A2	EXCLK_A2
ASW2	ASW2
PSW2	PSW2
FT_CLK	FT_CLK
FT_DATA0	FT_DATA0
FT_PROG	FT_PROG
FT_DONE	FT_DONE
X_M1	X_M1

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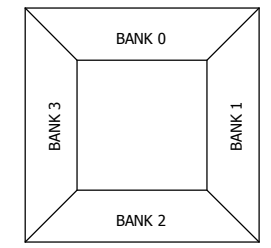


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 Date: 5-Apr-2012 16:23:49
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 Sheet 2 of 2

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SDP	8	9	SDP O
SC	7	10	SC O
SD	6	11	SD O
SE	5	12	SE O
SG	4	13	SG O
SF	3	14	SF O
SA	2	15	SA O
SB	1	16	SB O

