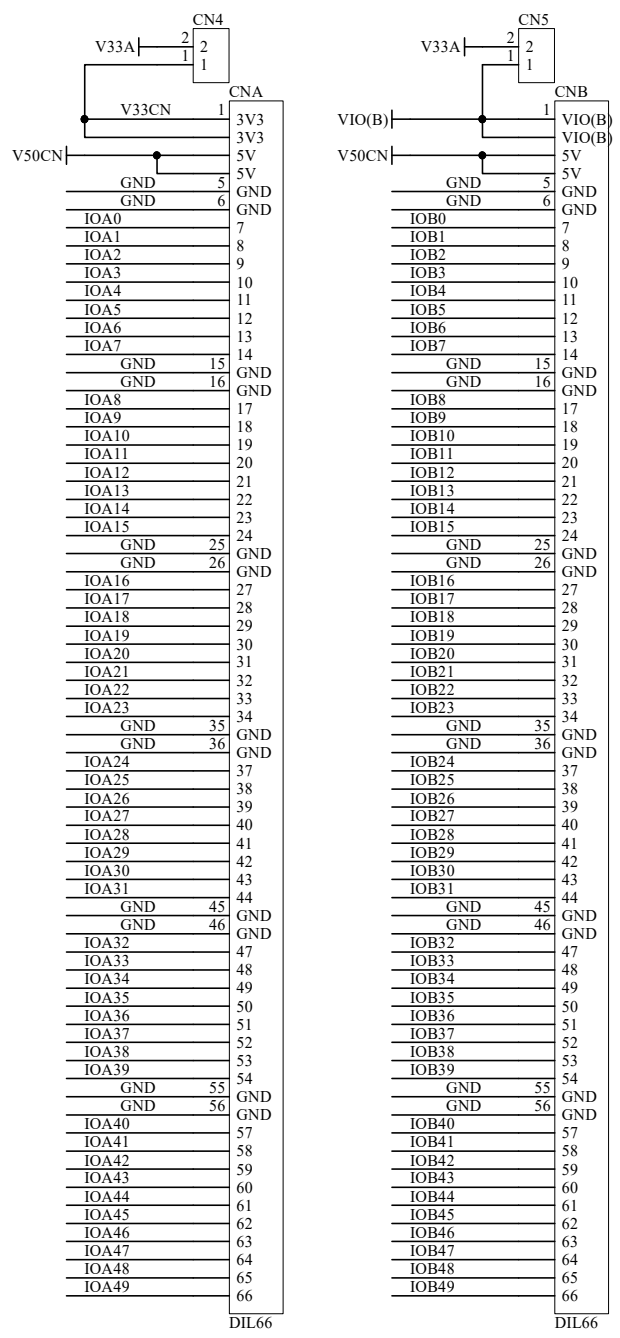
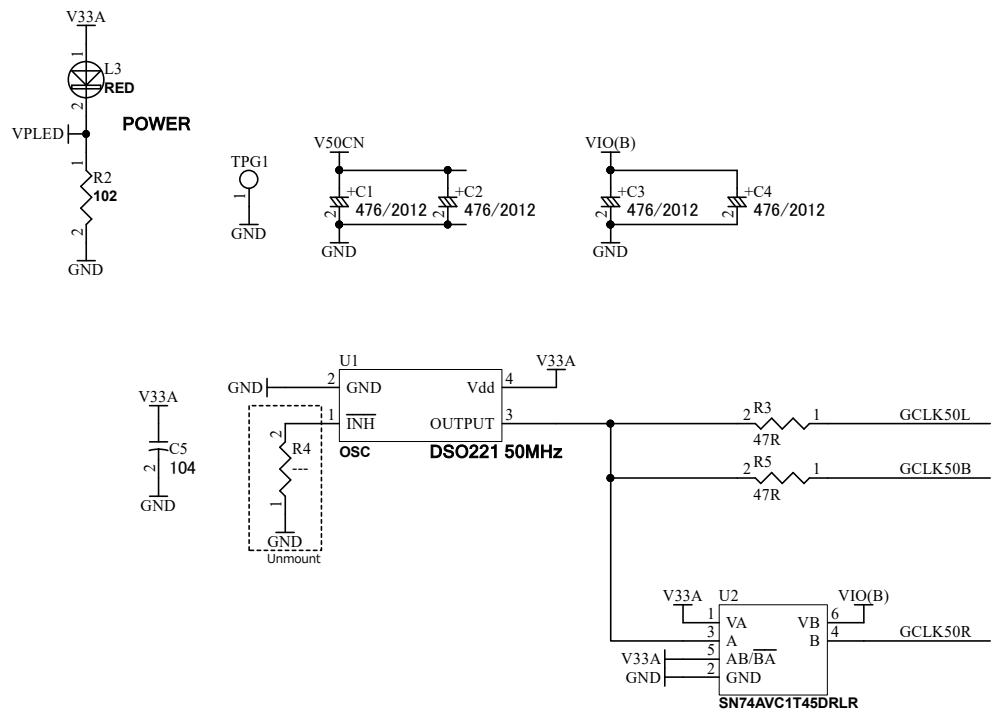
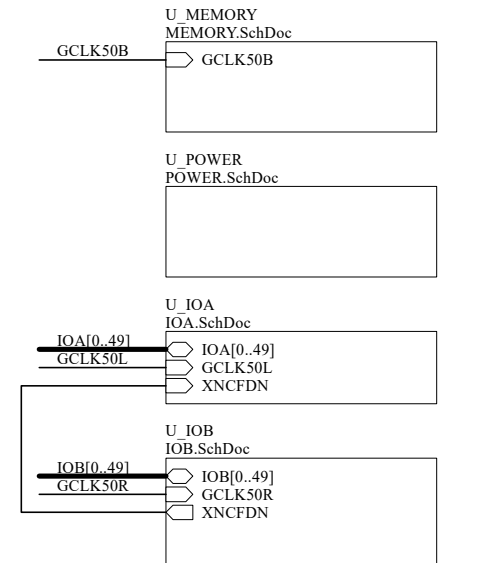


A

A



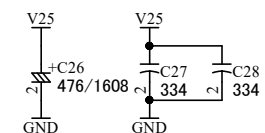
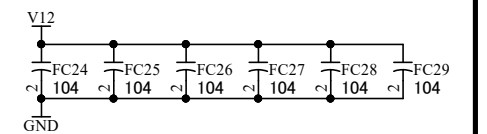
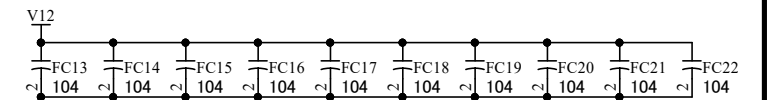
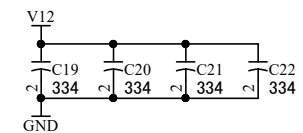
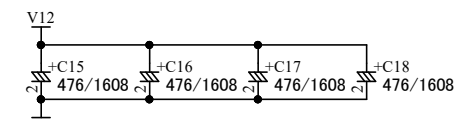
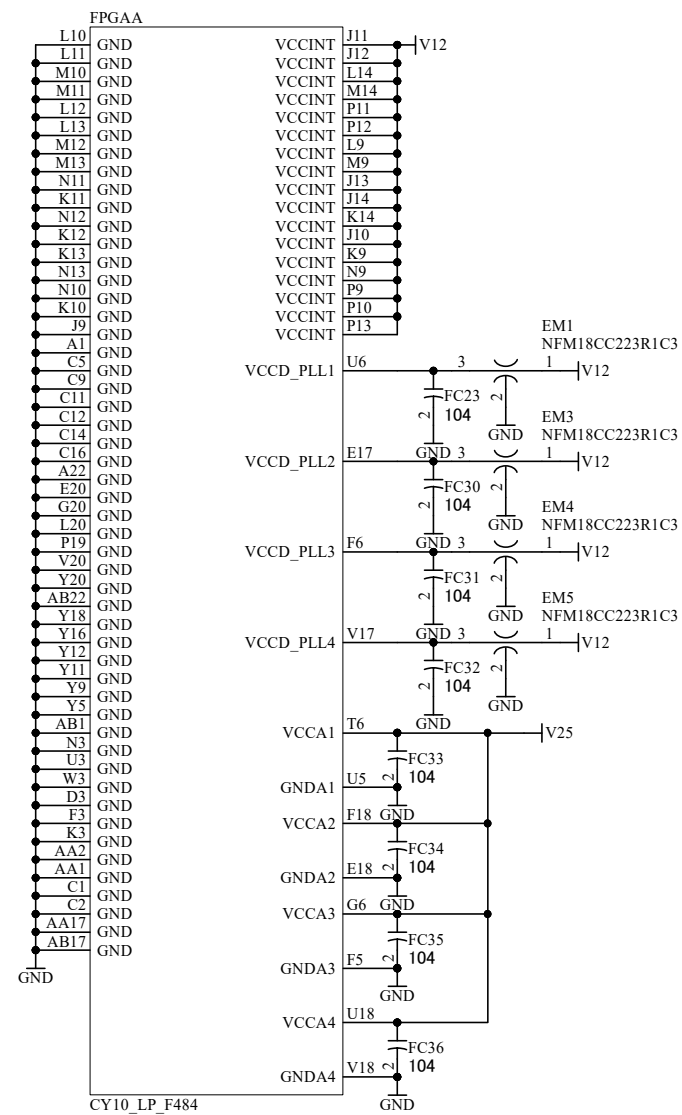
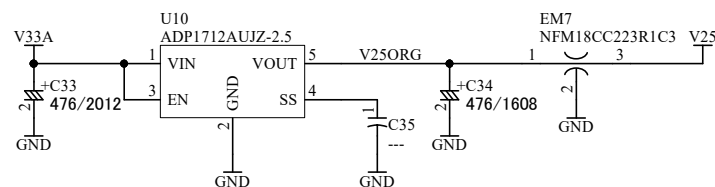
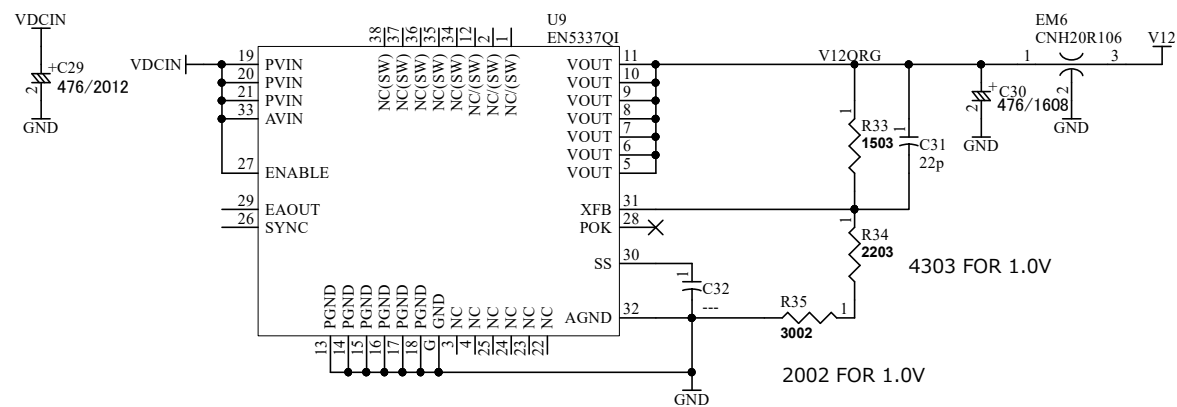
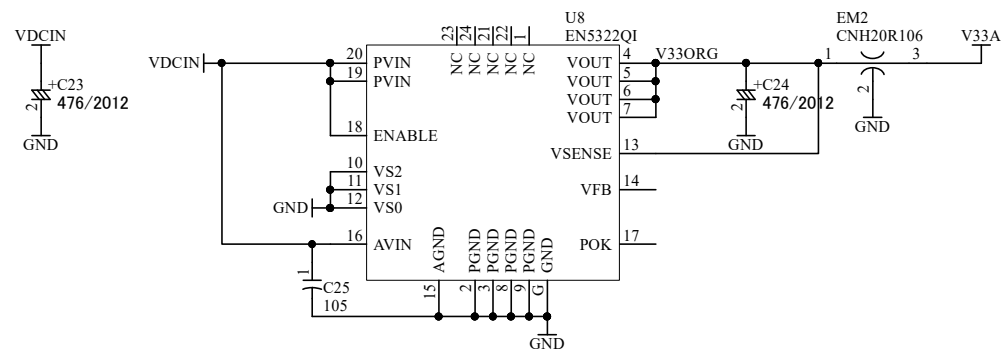
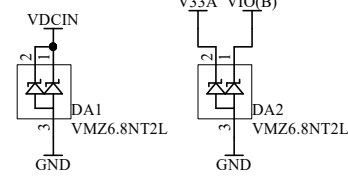
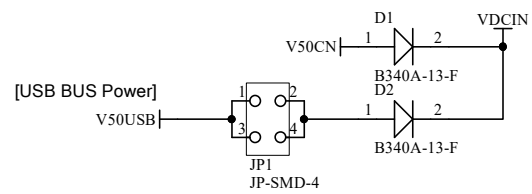
FPGAB		P14	
H3	IO_DIFFIO_L7n/B1(GND(040/016))	VCCINT(IO(016))	P14
J5	GND(IO(080/055/040))(GND(016))	VCCINT(IO(016))	N14
R3	IO_DIFFIO_L37n/B2(GND(040/016))	VCCINT(IO(016))	J16
AB6	IO_DIFFIO_B8p/B3(GND(040/016))	VCCINT(IO(016))	K15
Y15	IO_DIFFIO_B39n/B4(GND(040/016))	VCCINT(IO(016))	L16
T20	IO_DIFFIO_R45n/B5(GND(040/016))	VCCINT(IO(016))	M15
C18	IO_DIFFIO_T58n/B7(GND(040/016))	VCCINT(IO(016))	R12
D8	IO_DIFFIO_T19n/B8(GND(040/016))	VCCINT(IO(016))	R10
D7	IO_DIFFIO_T15p/B8(GND(016))	VCCINT(IO(016))	R8
Y21	GND(IO(080/055/040/016))	VCCINT(IO(016))	H9
U19	GND(IO(080/055/040/016))	VCCINT(IO(016))	G12
R18	GND(IO(080/055/040/016))	VCCINT(IO(016))	J8
J19	GND(IO(080/055/040/016))	VCCINT(IO(040/016))	M8
G7	GND(IO(080/055/040/016))	VCCINT(IO(040/016))	T7
		VCCINT(IO(040/016))	T9
		VCCINT(IO(040/016))	T13
F12	GND(IO(016))	VCCINT(IO(040/016))	P15
H12	GND(IO(016))	VCCINT(IO(040/016))	H15
H13	GND(IO(016))	VCCINT(IO(040/016))	H11
J15	GND(IO(016))	VCCINT(IO(040/016))	K8
K16	GND(IO(016))	VCCINT(IO(040/016))	P17
L15	GND(IO(016))	VCCINT(IO(055/040/016))	L7
N15	GND(IO(016))	VCCINT(IO(040/016))	N16
R13	GND(IO(016))	VCCINT(IO(055/040/016))	K17
R11	GND(IO(016))	VCCINT(IO(055/040/016))	J17
R9	GND(IO(016))	VCCINT(IO(055/040/016))	G16
P8	GND(IO(016))	VCCINT(IO(055/040/016))	G14
H14	GND(IO(040/016))	VCCINT(IO(055/040/016))	G10
H10	GND(IO(040/016))	VCCINT(IO(055/040/016))	G8
H8	GND(IO(040))(GND(016))	VCCINT(IO(055/040/016))	J7
N8	GND(IO(040/016))	VCCINT(IO(055/040/016))	N7
R7	GND(IO(040/016))	VCCINT(IO(055/040/016))	P7
T8	GND(IO(040/016))	VCCINT(IO(055/040/016))	R6
T12	GND(IO(040/016))	VCCINT(IO(055/040/016))	U8
P16	GND(IO(040/016))	VCCINT(IO(055/040/016))	V7
L8	GND(IO(040/016))	VCCINT(IO(055/040/016))	T11
G17	GND(IO(055/040/016))	VCCINT(IO(055/040/016))	R15
M7	GND(IO(055/040/016))	VCCINT(IO(055/040/016))	G4
F16	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	U15
H16	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	U16
G15	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	U17
G13	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	R14
G11	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	H17
E10	GND(IO(055/040/016))		
G9	GND(IO(055/040/016))		
K7	GND(IO(055/040/016))		
P6	GND(IO(055/040/016))		
U7	GND(IO(055/040/016))		
V6	GND(IO(055/040/016))		
T10	GND(IO(055/040/016))		
U13	GND(IO(055/040/016))		
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N17	GND(IO(055/040/016))		
GND	CY10_LP_F484		



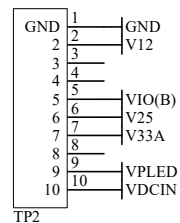
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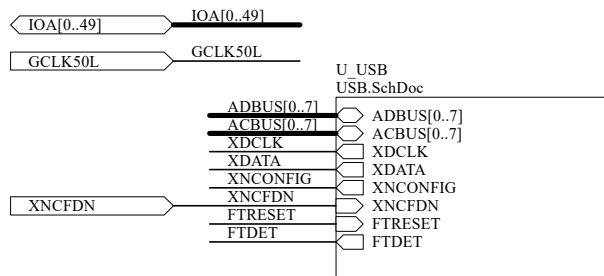
Power sense point



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DSN:	TITLE: Intel Cyclone 10 LP F484 USB FPGA Board
DOC. No:	<b>EDA-011</b>
FILE: POWER.SchDoc	DATE: 2018/02/26 9:57:55
Sheet:	<b>B</b>



ClassName: FIXED  
 ClassName: FIXED

FPGAJ	
A11	CLK10_DIFFCLK_4n/B8
B11	CLK11_DIFFCLK_4p/B8
E6	IO_PLL3_CLKOUTn/B8
E5	IO_PLL3_CLKOUTp/B8
A10	IO_DIFFIO_T30n/B8
B10	IO_DIFFIO_T30p/B8
A9	IO_DIFFIO_T29n/B8
B9	IO_DIFFIO_T29p/B8
A8	IO_DIFFIO_T25n/B8
B8	IO_DATA3_DIFFIO_T25p/B8
A7	IO_DIFFIO_T23n/B8
B7	IO_DATA4_DIFFIO_T23p/B8
A6	IO_DIFFIO_T22n/B8
B6	IO_DIFFIO_T22p/B8
C8	IO_DIFFIO_T20n/B8
C7	IO_DIFFIO_T20p/B8
A4	IO_DIFFIO_T14n/B8
B4	IO_DIFFIO_T14p/B8
A3	IO_DIFFIO_T9n/B8
B3	IO_DIFFIO_T9p/B8
C3	IO_DIFFIO_T4n/B8
C4	IO_DIFFIO_T4p/B8
D10	IO_DIFFIO_T31n/B8
A5	IO_DATA5_DIFFIO_T18p/B8
F10	IO_DATA6_DIFFIO_T17p/B8
C6	IO_DATA7_DIFFIO_T15n/B8
F8	IO_DIFFIO_T11n/B8
E7	IO_DIFFIO_T7n/B8(IO(040/016))
F7	IO_DIFFIO_T3n/B8
F9	IO_B8(IO(016))
C10	IO_VREFB8N0/B8(IO(016))
E9	IO_DIFFIO_T21n/B8(IO_VREFB(040/016))
B5	IO_VREFB8N1/B8(IO(016))
D6	IO_VREFB8N2/B8(IO(055))
E8	IO_DIFFIO_T19p/B8(VCCIO8(040/016))
A2	VCCIO8
D5	VCCIO8
D9	VCCIO8
D11	VCCIO8

ClassName: FIXED

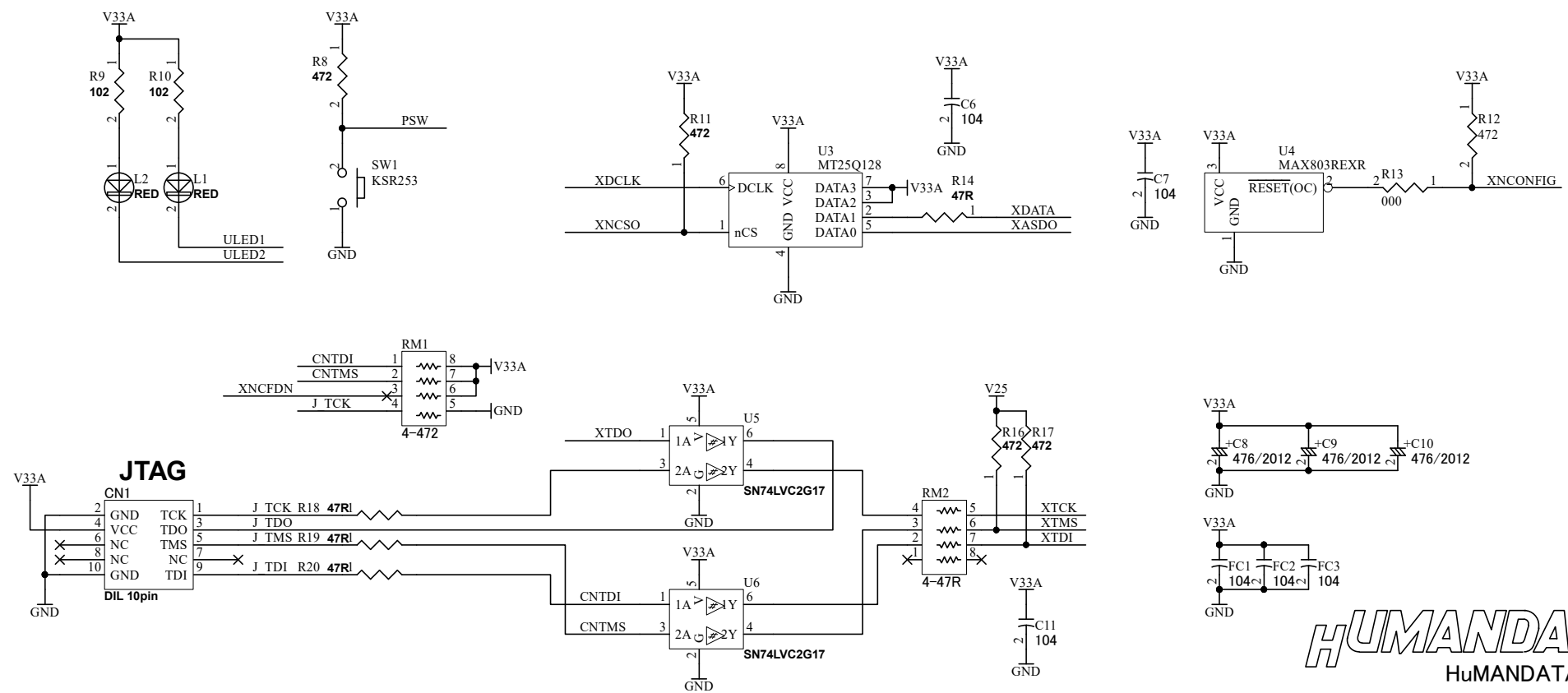
FPGAJ		FPGA I	
IOA0	A20	IO_PLL2_CLKOUTn/B7	A12
IOA1	B20	IO_PLL2_CLKOUTp/B7	B12
ACBUS6	E16	IO_DIFFIO_T60n/B7	GND
ACBUS7	F15	IO_DIFFIO_T60p/B7	
ACBUS0	C19	IO_DIFFIO_T56n/B7	
ACBUS2	D19	IO_DIFFIO_T56p/B7	
ADBUS4	A18	IO_DIFFIO_T53n/B7	
ADBUS6	B18	IO_DIFFIO_T53p/B7	
ADBUS3	A17	IO_DIFFIO_T50n/B7	
ADBUS5	B17	IO_DIFFIO_T50p/B7	
ADBUS1	A16	IO_DIFFIO_T49n/B7	
ADBUS2	B16	IO_DIFFIO_T49p/B7	
ACBUS4	E14	IO_DIFFIO_T46n/B7	
ACBUS1	F13	IO_DIFFIO_T46p/B7	
ADBUS0	A15	IO_DIFFIO_T45n/B7	
	B15	IO_DIFFIO_T45p/B7	
IOA12	C13	IO_DIFFIO_T44n/B7	
IOA13	D13	IO_DIFFIO_T44p/B7	
IOA3	A14	IO_DIFFIO_T36n/B7	
IOA2	B14	IO_DIFFIO_T36p/B7	
	A13	IO_DIFFIO_T35n/B7	
ACBUS5	B13	IO_DIFFIO_T35p/B7	
FTRESET	E11	IO_DIFFIO_T32n/B7	
FTDET	F11	IO_DIFFIO_T32p/B7	
	F14	IO_DIFFIO_T59p/B7	
ADBUS7	C17	IO_DIFFIO_T54p/B7(IO(016))	
	E15	IO_DIFFIO_T52p/B7	
	E12	IO_DIFFIO_T33p/B7(IO(080/055))(IO(016))	
	B19	IO_RUP4/B7	
	A19	IO_RDN4/B7	
ACBUS3	D17	IO_VREFB7N0/B7	
IOA11	D15	IO_DIFFIO_T52n/B7(IO_VREFB(040))(IO(016))	
IOA10	C15	IO_VREFB7N1/B7	
	E13	IO_VREFB7N2/B7(IO(055/016))	
	D18	IO_DIFFIO_T58p/B7(VCCIO7(040/016))	
	A21	VCCIO7	
	D12	VCCIO7	
	D14	VCCIO7	
	D16	VCCIO7	

TOP

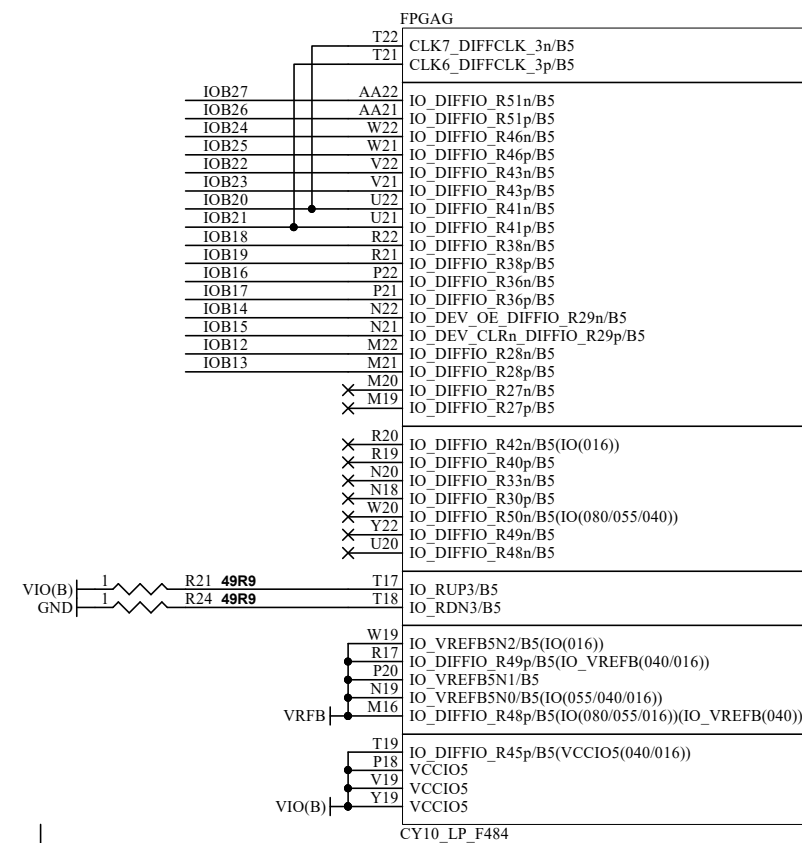
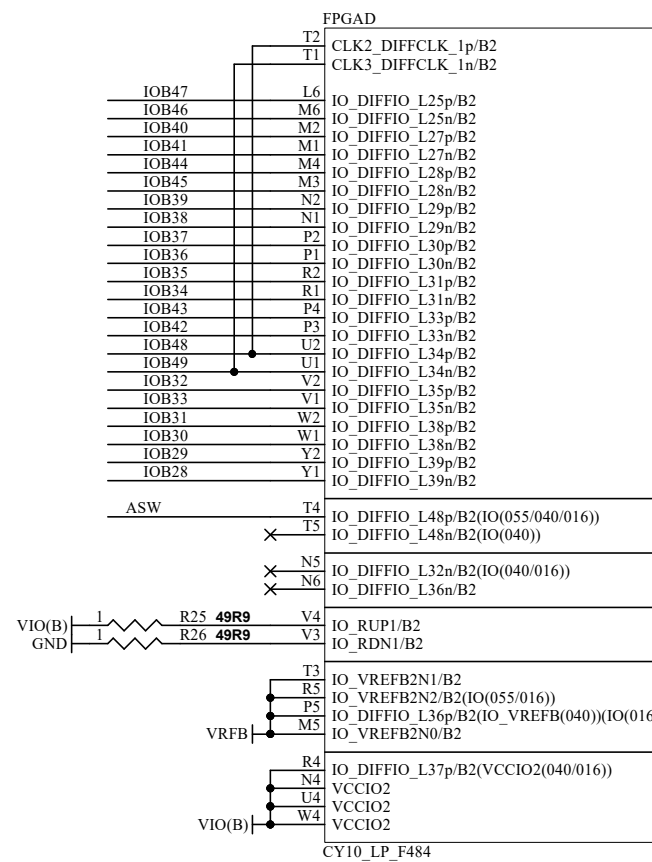
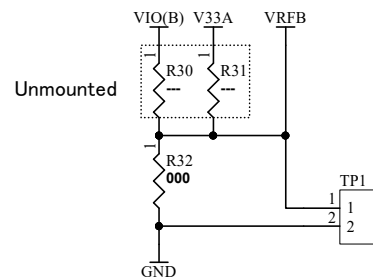
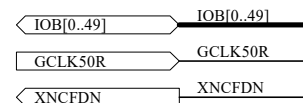
LEFT

FPGA G		FPGA C	
GCLK50L	G2	CLK0_DIFFCLK_0p/B1	G1
	G1	CLK1_DIFFCLK_0n/B1	
IOA29	B2	IO_DIFFIO_L2p/B1	
IOA28	B1	IO_DIFFIO_L2n/B1	
IOA42	E4	IO_DIFFIO_L3p/B1	
IOA43	E3	IO_DIFFIO_L3n/B1	
IOA44	D2	IO_DIFFIO_L5p/B1	
XASDO	D1	IO_DATA1_ASDO_DIFFIO_L5n/B1	
PSW	H6	IO_DIFFIO_L6p/B1	
XNCSO	J6	IO_DIFFIO_L6n/B1	
IOA45	E1	IO_FLASH_nCE_nCSO_DIFFIO_L8p/B1	
IOA31	F2	IO_DIFFIO_L8n/B1	
IOA30	F1	IO_DIFFIO_L9p/B1	
IOA33	H2	IO_DIFFIO_L9n/B1	
IOA32	H1	IO_DIFFIO_L13p/B1	
IOA35	J2	IO_DIFFIO_L13n/B1	
IOA34	J1	IO_DIFFIO_L23p/B1	
		IO_DIFFIO_L23n/B1	
	G3	IO_DIFFIO_L1n/B1	
	J4	IO_DIFFIO_L12p/B1(IO(040/016))	
XDCLK	K2	IO_DCLK/B1	
XDATA	K6	nSTATUS/B1	
XNCONFIG	K1	IO_DATA0/B1	
	K5	nCONFIG/B1	
XTDI	L5	TDI/B1	
XTCK	L2	TCK/B1	
XTMS	L1	TMS/B1	
XTDO	L4	TDO/B1	
	L3	nCE/B1	
	G5	IO_VREFB1N0/B1(IO(016))	
	H7	IO_DIFFIO_L1p/B1(IO(080/055))(IO_VREFB(040/016))	
	H5	IO_VREFB1N1/B1(IO(016))	
	J3	IO_VREFB1N2/B1(IO(055))	
IOA47	H4	IO/B1(IO(080/055))(VCCIO1(040/016))	
	D4	VCCIO1	
	F4	VCCIO1	
	K4	VCCIO1	

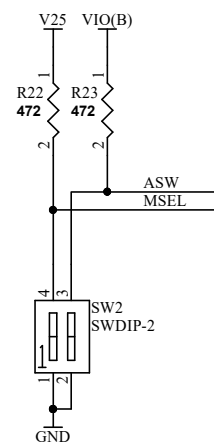
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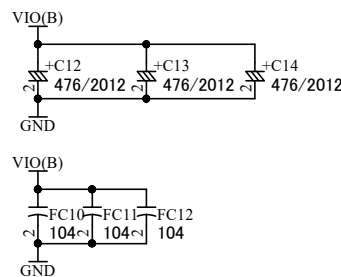
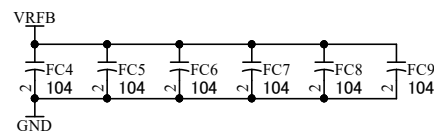
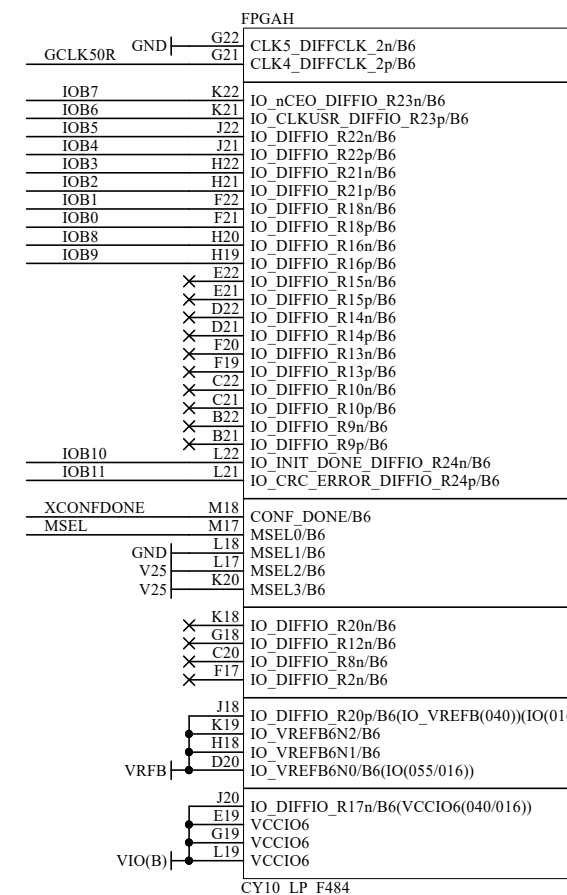
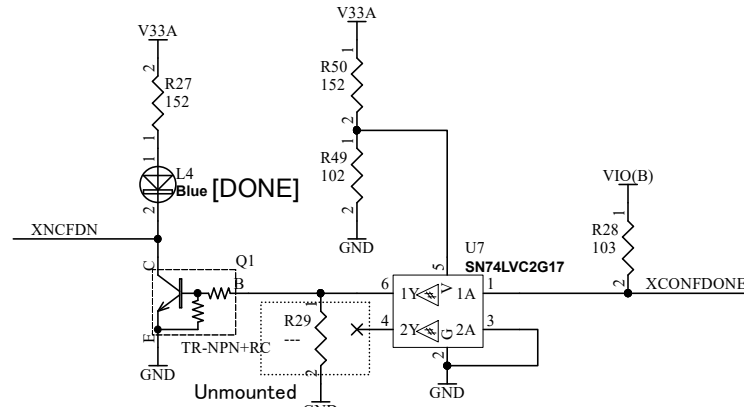
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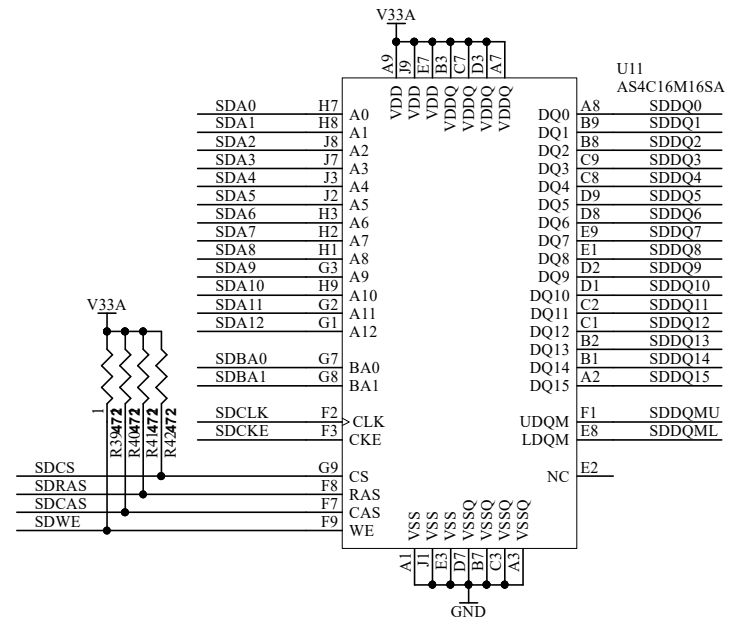
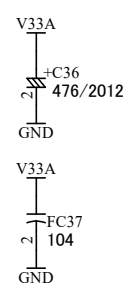
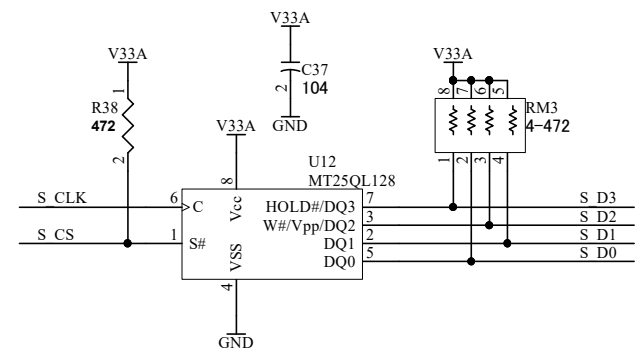
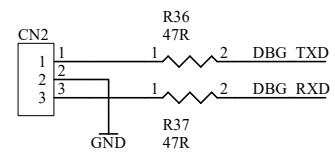
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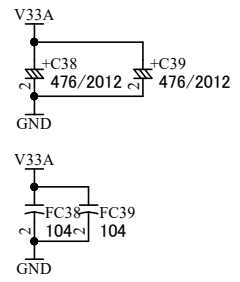
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GCLK50B GCLK50B



GCLK50B		FPGA E	
GND	AA11	CLK15_DIFFCLK	6p/B3
	AB11	CLK14_DIFFCLK	6n/B3
DBG RXD	AA3	IO_PLL1_CLKOUTp/B3	
DBG TXD	AB3	IO_PLL1_CLKOUTn/B3	
SDA5	W7	IO_DIFFIO_B9p/B3	
SDDQ8	Y7	IO_DIFFIO_B9n/B3	
SDDQ10	AA7	IO_DIFFIO_B14p/B3	
SDDQ9	AB7	IO_DIFFIO_B14n/B3	
SDDQ12	AA8	IO_DIFFIO_B17p/B3	
SDDQ11	AB8	IO_DIFFIO_B17n/B3	
SDDQ15	AA9	IO_DIFFIO_B18p/B3	
SDDQ14	AB9	IO_DIFFIO_B18n/B3	
SDA9	W10	IO_DIFFIO_B23p/B3	
	Y10	IO_DIFFIO_B23n/B3	
S D1	V8	IO_DIFFIO_B13p/B3	
SDA4	W8	IO_DIFFIO_B13n/B3(IO(080/055/040/016))	
SDA6	V10	IO_DIFFIO_B15p/B3(IO(016))	
S D0	U10	IO_DIFFIO_B15n/B3	
SDDQ0	AA10	IO_DIFFIO_B24p/B3	
SDDQ13	AB10	IO_DIFFIO_B24n/B3(IO(016))	
SDA8	Y3	IO_DIFFIO_B3n/B3	
SDA7	W6	IO_DIFFIO_B4p/B3	
SDA11	AA5	IO_DIFFIO_B5p/B3	
SDDQMU	AB5	IO_DIFFIO_B8n/B3	
S CLK	V5	IO_DIFFIO_B1n/B3	
S CS	Y6	IO/B3(IO(040/016))	
SDA12	AA4	IO/B3(IO(016))	
S D3	U9	IO_DIFFIO_B12n/B3	
S D2	Y8	IO/B3(IO(080/055/040/016))	
SDCKE	V11	IO/B3(IO(055/040/016))	
	V9	IO_VREFB3N1/B3	
	U11	IO_VREFB3N0/B3(IO(055/016))	
	Y4	IO_DIFFIO_B3p/B3(IO_VREFB(040/016))	
	AB4	IO_VREFB3N2/B3(IO(016))	
	AA6	IO_DIFFIO_B7n/B3(VCCIO3(040/016))	
	AB2	VCCIO3	
	W5	VCCIO3	
	W9	VCCIO3	
	W11	VCCIO3	

GCLK50B		FPGA F	
GND	AA12	CLK13_DIFFCLK	7p/B4
	AB12	CLK12_DIFFCLK	7n/B4
SDCLK	T16	IO_PLL4_CLKOUTp/B4	
	R16	IO_PLL4_CLKOUTn/B4	
SDDQ2	AA13	IO_DIFFIO_B32p/B4	
SDDQ1	AB13	IO_DIFFIO_B32n/B4	
SDDQ3	AA14	IO_DIFFIO_B35p/B4	
SDDQ4	AB14	IO_DIFFIO_B35n/B4	
SDCAS	W13	IO_DIFFIO_B36p/B4	
SDA2	Y13	IO_DIFFIO_B36n/B4	
SDDQ5	AA15	IO_DIFFIO_B37p/B4	
SDDQ6	AB15	IO_DIFFIO_B37n/B4	
SDDQ7	AA16	IO_DIFFIO_B40p/B4	
SDDQML	AB16	IO_DIFFIO_B40n/B4	
SDBA0	U14	IO_DIFFIO_B44p/B4	
SDA0	V15	IO_DIFFIO_B44n/B4	
SDA10	W17	IO_DIFFIO_B48p/B4	
	Y17	IO_DIFFIO_B48n/B4	
SDCS	AA20	IO_DIFFIO_B49p/B4	
SDWE	AB20	IO_DIFFIO_B49n/B4	
SDBA1	V13	IO_DIFFIO_B41p/B4(IO(040/016))	
	V14	IO_DIFFIO_B43p/B4	
SDA1	W15	IO_DIFFIO_B45p/B4	
	T15	IO_DIFFIO_B46n/B4	
SDRAS	AB18	IO/B4	
SDA3	U12	IO_DIFFIO_B38p/B4	
	AA19	IO_RUP2/B4	
	AB19	IO_RDN2/B4	
	V12	IO_VREFB4N2/B4(IO(016))	
	W14	IO_DIFFIO_B41n/B4(IO_VREFB(040/016))	
	AA18	IO_VREFB4N1/B4(IO(016))	
	V16	IO_VREFB4N0/B4(IO(055))	
	Y14	IO_DIFFIO_B39p/B4(VCCIO4(040/016))	
	AB21	VCCIO4	
	W12	VCCIO4	
	W16	VCCIO4	
	W18	VCCIO4	

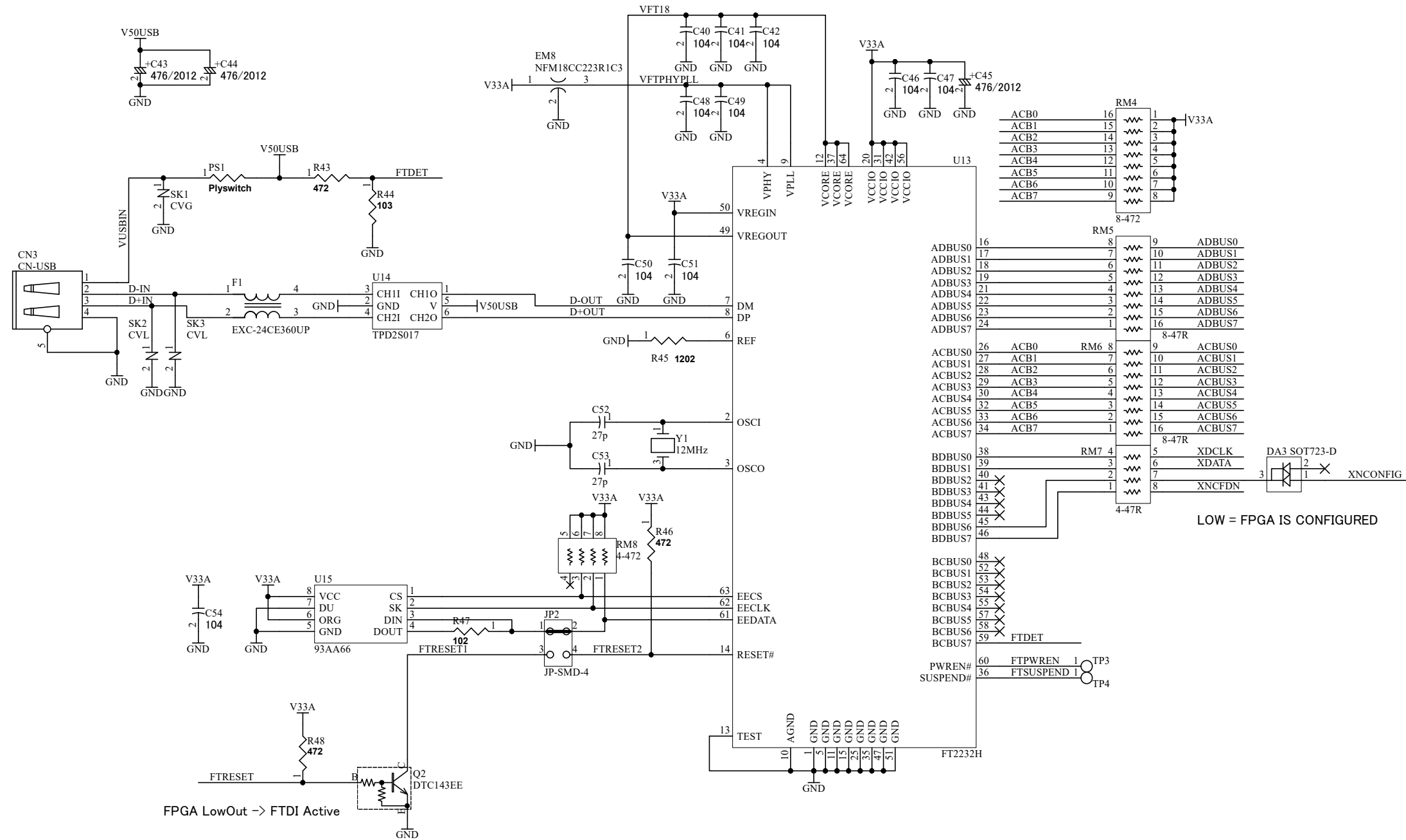


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ADBUS[0..7]	ADBUS[0..7]
ACBUS[0..7]	ACBUS[0..7]
XDCLK	XDCLK
XDATA	XDATA
XNCONFIG	XNCONFIG
XNCFDN	XNCFDN
FTDET	FTDET
FTRESET	FTRESET



FPGA LowOut -> FTDI Active

LOW = FPGA IS CONFIGURED

DSN:	TITLE: Intel Cyclone 10 LP F484 USB FPGA Board
DOC. No:	<b>EDA-011</b>
FILE: USB.SchDoc	DATE: 2018/02/26 9:57:56
Sheet: 6 / 6	<b>B</b>