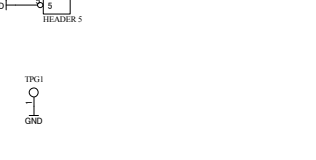
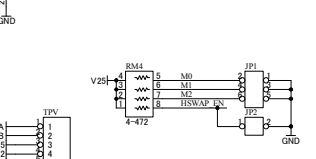
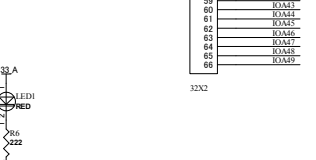
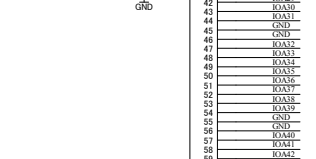
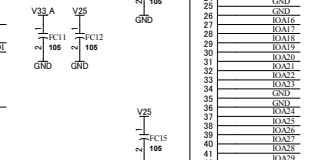
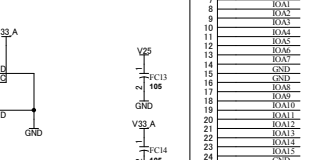
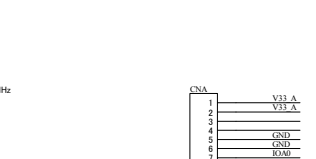
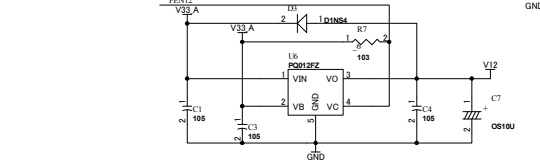
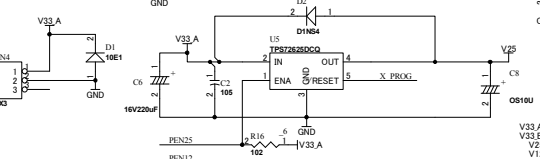
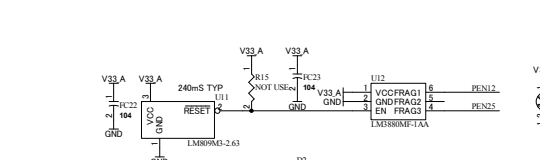
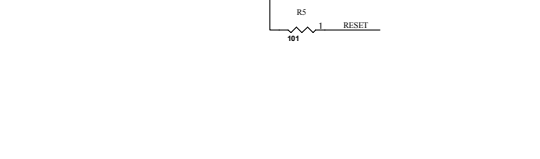
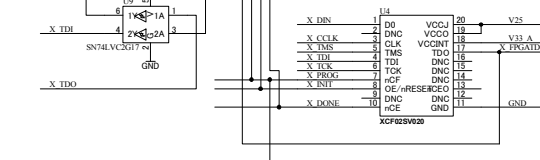
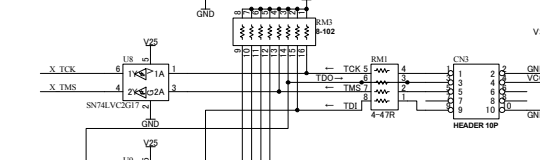
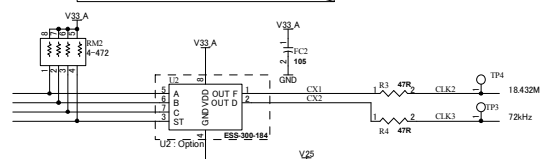
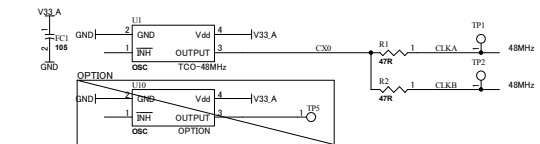
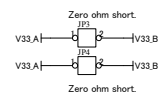
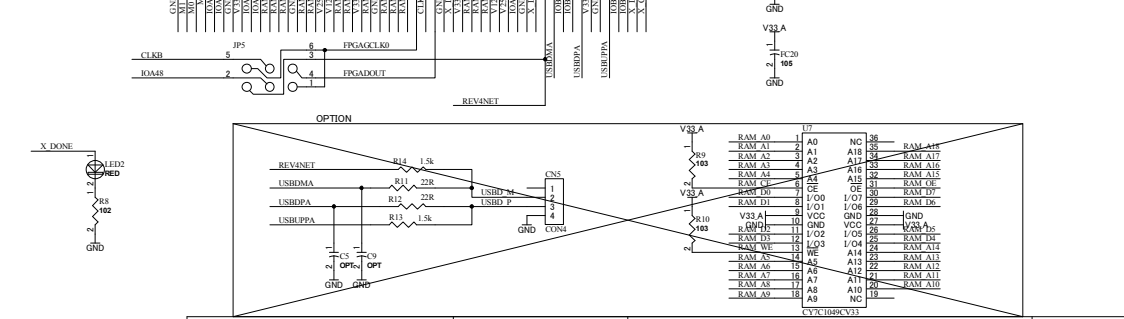
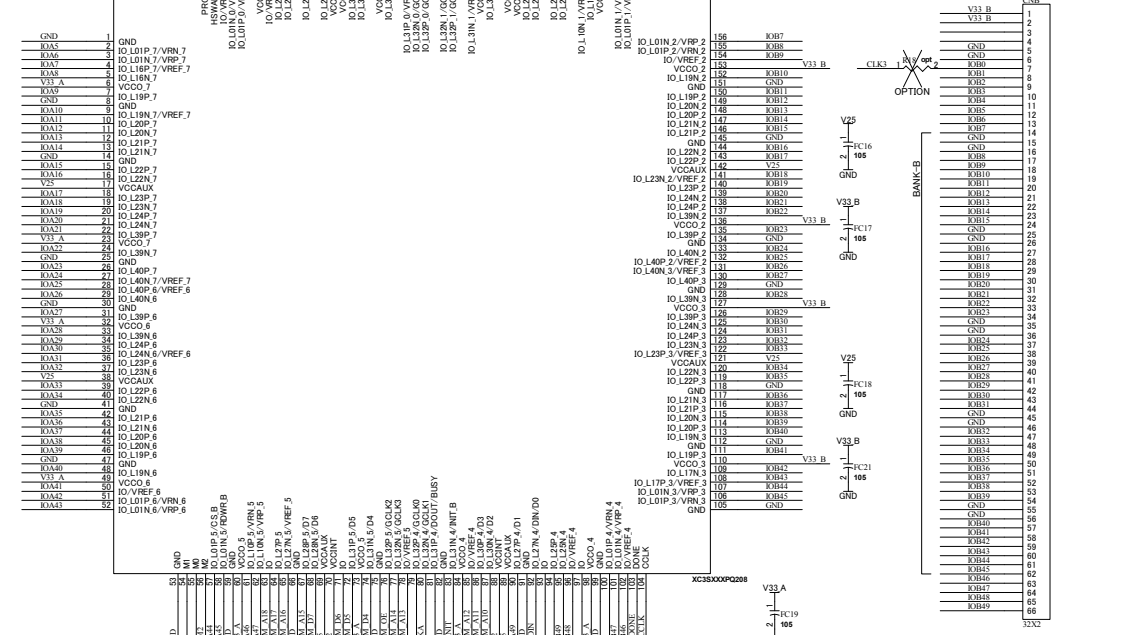
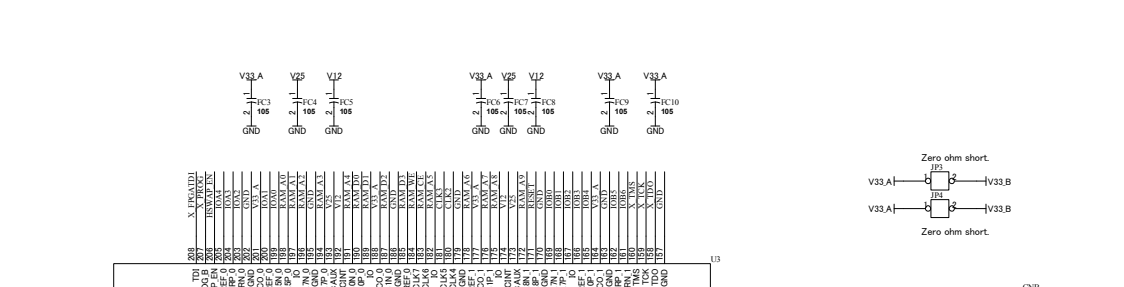


V12
V25
V33 A
V33 B
GND



CNA	V33 A
1	V33 A
2	V33 A
3	GND
4	GND
5	GND
6	GND
7	GND
8	GND
9	GND
10	GND
11	GND
12	GND
13	GND
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62	GND
63	GND
64	GND
65	GND
66	GND

CNA	V33 A
1	GND
2	GND
3	GND
4	GND
5	GND
6	GND
7	GND
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66	GND



	2010/05/11	SP3 FPGA BOARD(Rev.4)	
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Date: 11-May-2010	14:46:48	File: XCM001H.sch	Sheet 1 of 1