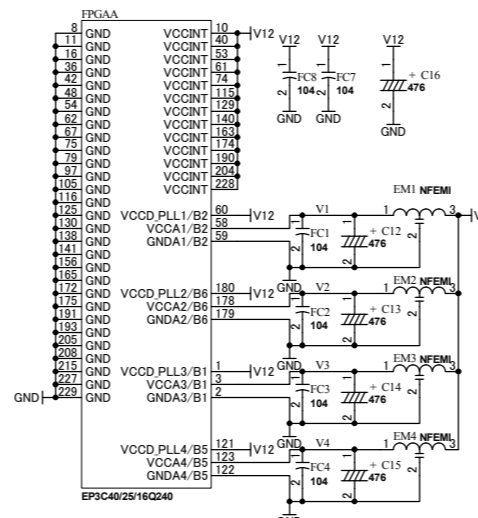
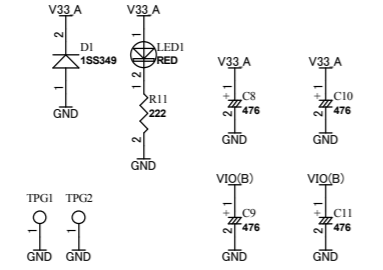
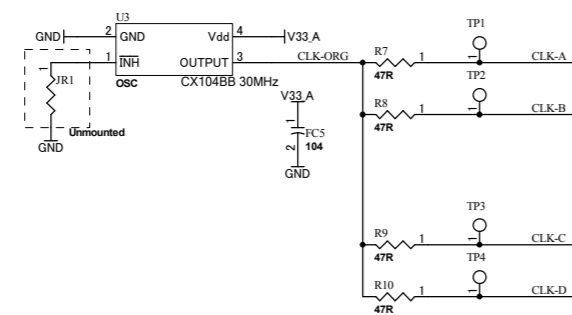
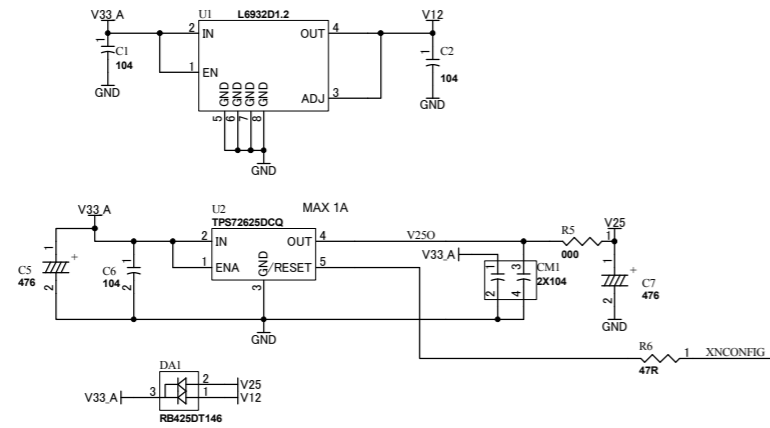
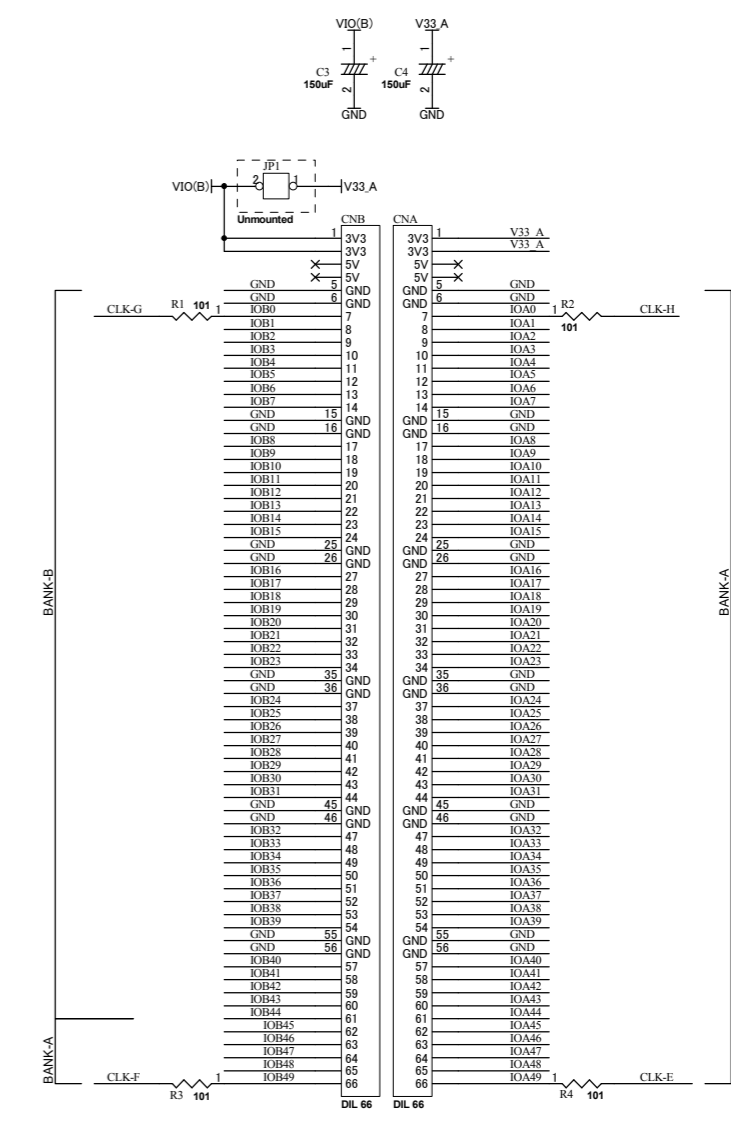


V33_A | V33_A
 VIO(B) | VIO(B)
 V12 | V12
 V25 | V25
 GND | GND



FPGACY3	
FPGACY3.sch	
IOA0-49	IOA[0..49]
IOB0-49	IOB[0..49]
CLK-A	CLK-A
CLK-B	CLK-B
CLK-C	CLK-C
CLK-D	CLK-D
CLK-E	CLK-E
CLK-F	CLK-F
CLK-G	CLK-G
CLK-H	CLK-H
XNCONFIG	XNCONFIG



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Altera CycloneIII Q240 FPGA board

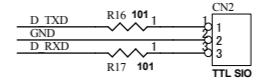
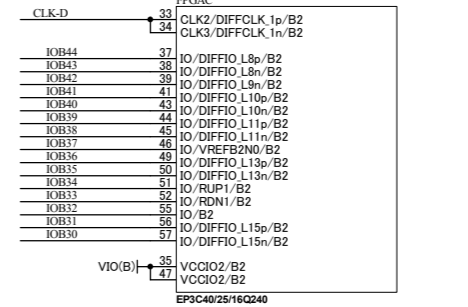
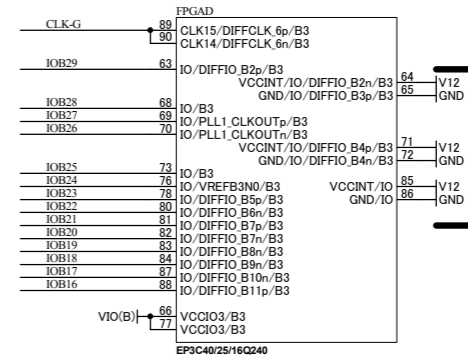
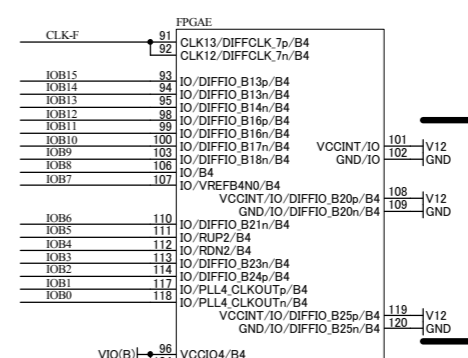
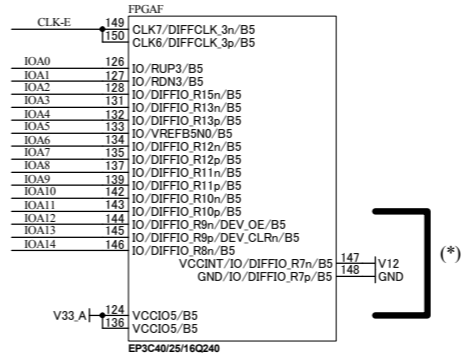
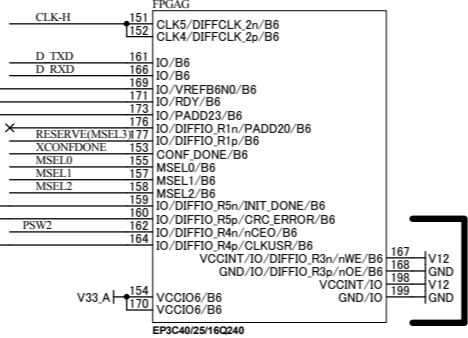
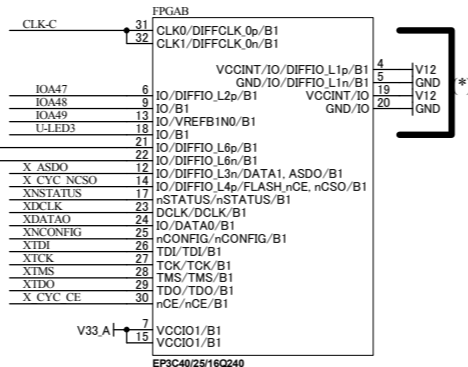
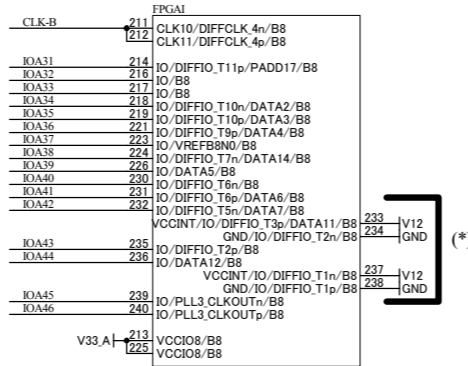
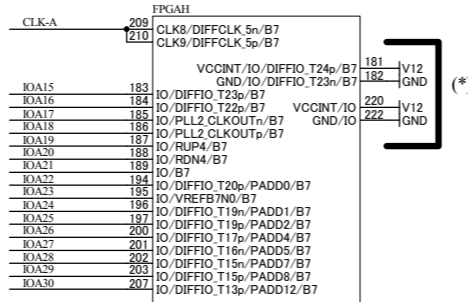
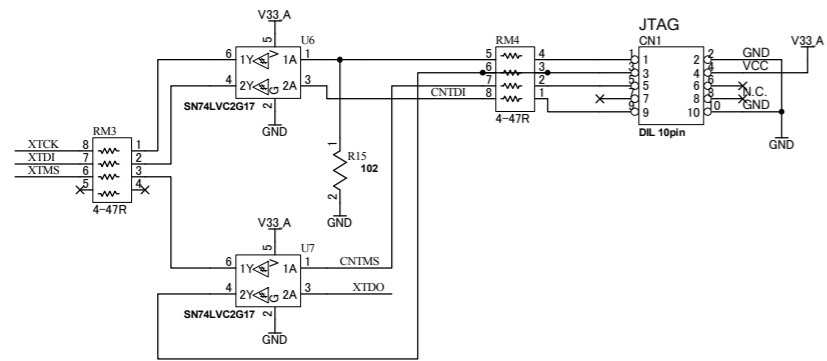
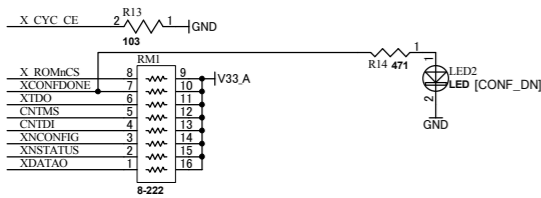
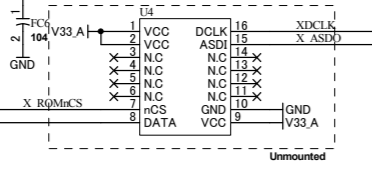
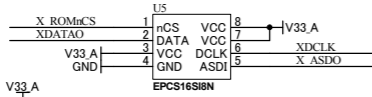
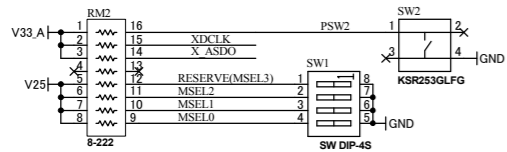
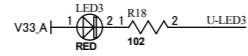
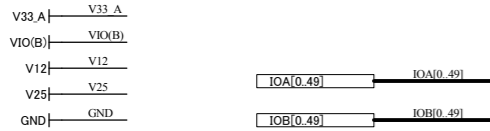
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D3

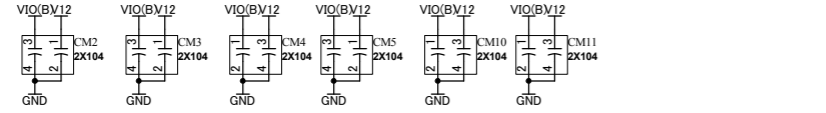
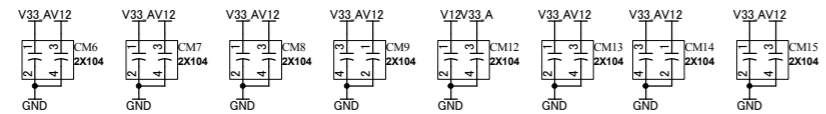
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File: ACM018D3.sch

Sheet 1 of 2



(*) These pins are connected to GND or VCCINT. You need to set them as INPUT.



		Altera CycloneIII Q240 FPGA board	
		DOC. No.	ACM-018
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