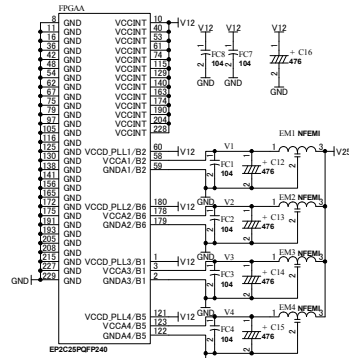
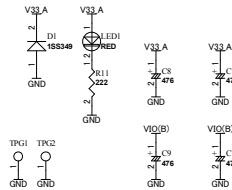
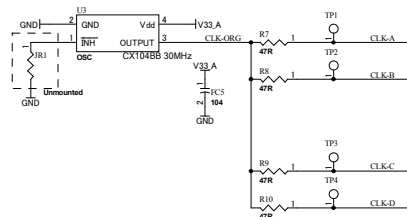
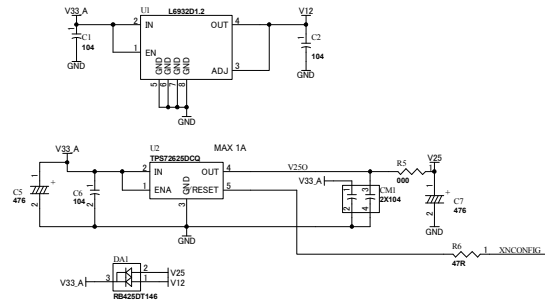
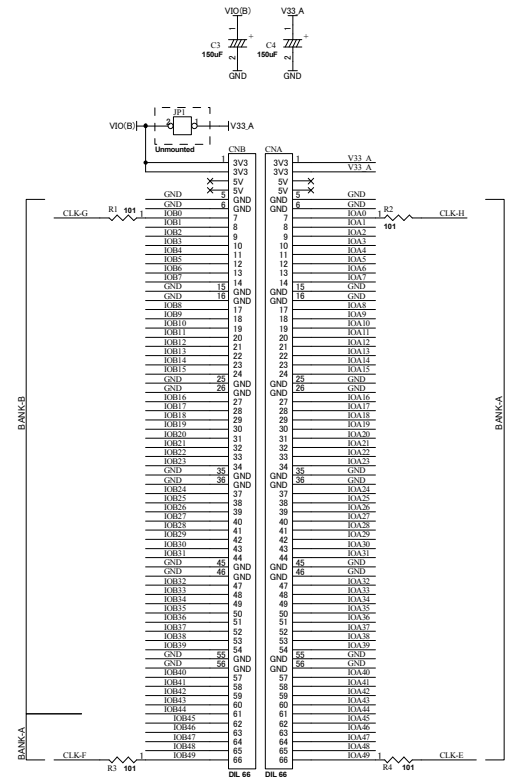


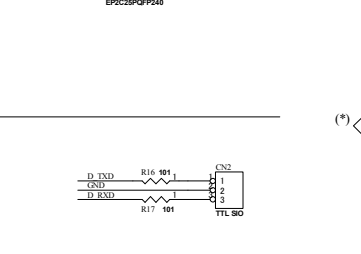
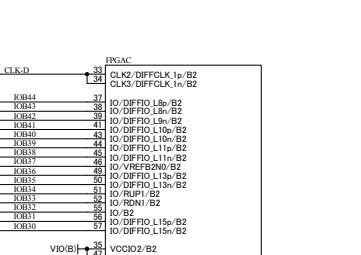
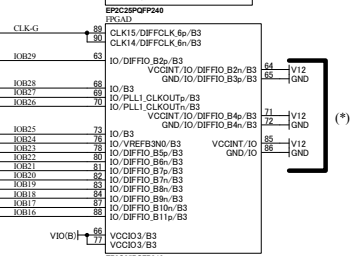
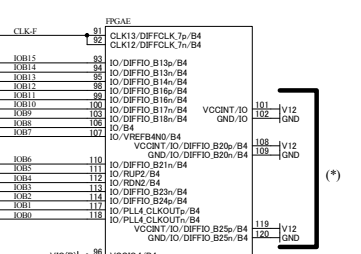
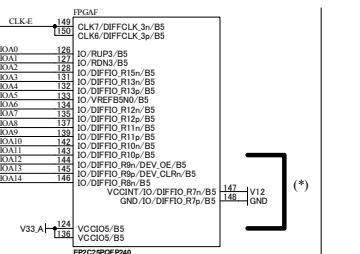
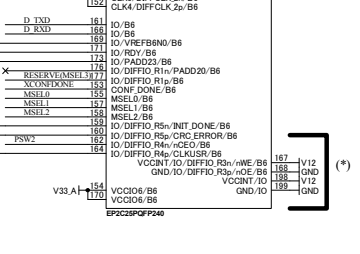
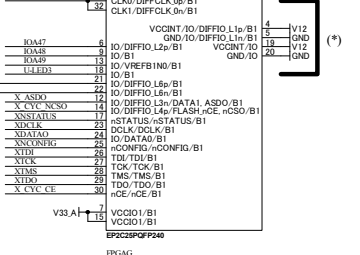
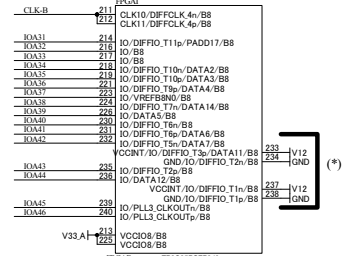
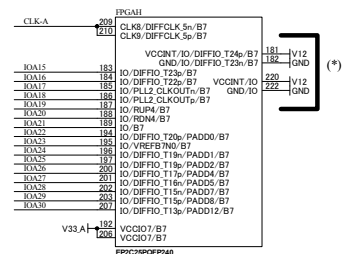
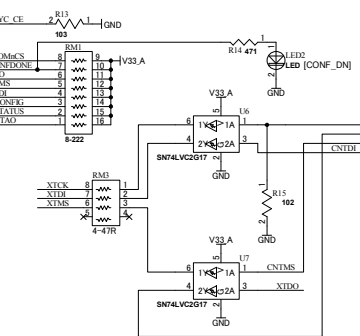
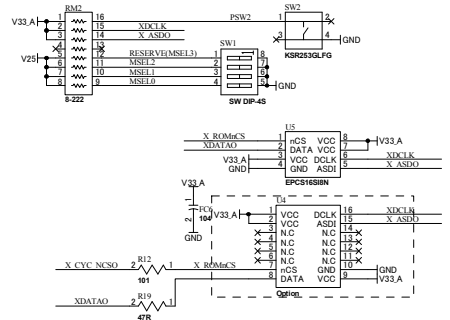
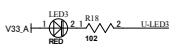
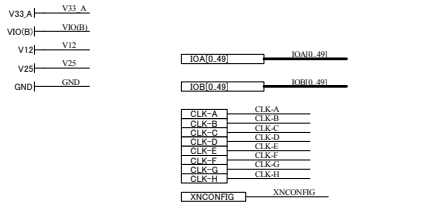
V33.A | V33.A  
 V10(B) | V10(B)  
 V12 | V12  
 V25 | V25  
 GND | GND



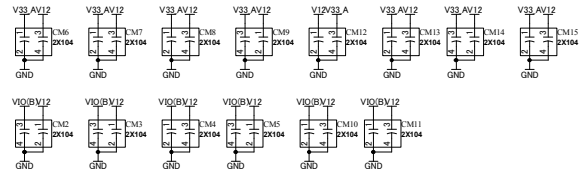
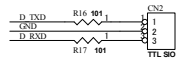
FPGA Pin	FPGA V33.A
IOA[0..49]	IOA[0..49]
IOB[0..49]	IOB[0..49]
CLK.A	CLK.A
CLK.B	CLK-B
CLK.C	CLK-C
CLK.D	CLK-D
CLK.E	CLK-E
CLK.F	CLK-F
CLK.G	CLK-G
CLK.H	CLK-H
XNCONF0	XCNC0CFG
XNCONF1	XCNC1CFG



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(\* ← These pins are connected to GND or VCCINT. You need to set them as INPUT.



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Altera CycloneIII Q240 FPGA board

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