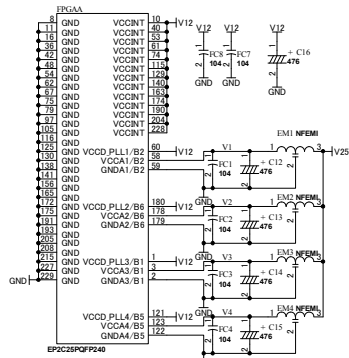
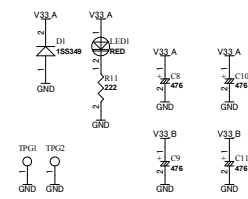
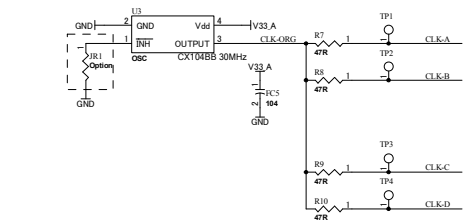
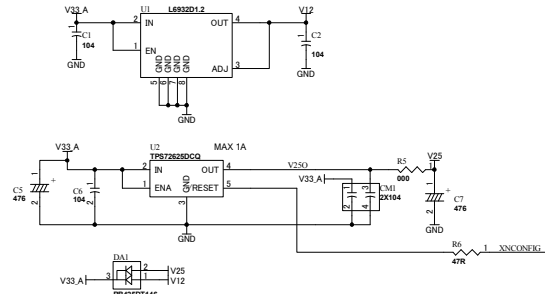
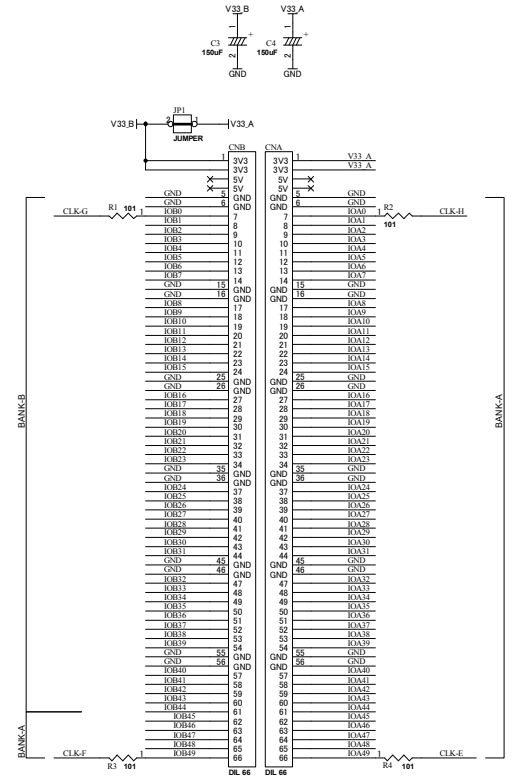


V33] V33
 V33.A] V33.A
 V33.B] V33.B
 V12] V12
 V25] V25
 GND] GND

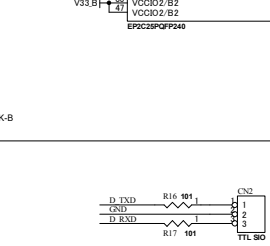
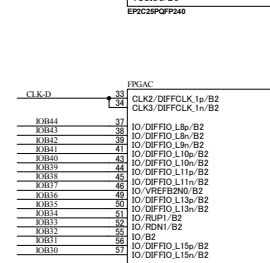
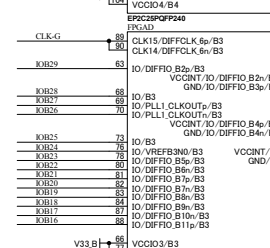
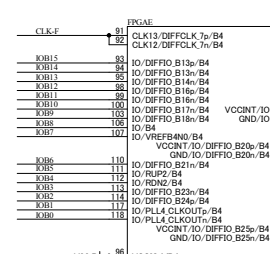
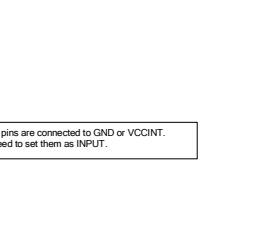
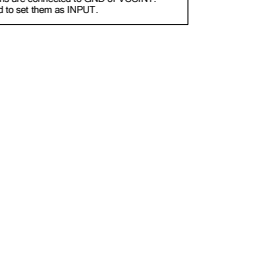
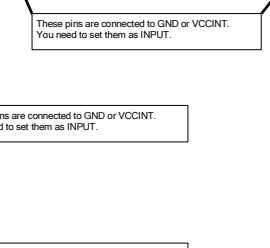
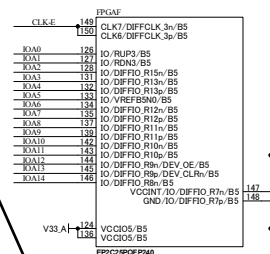
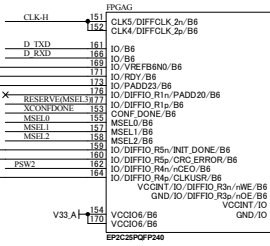
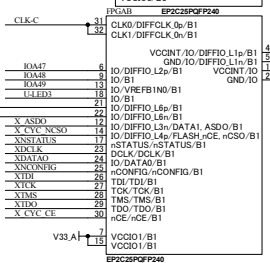
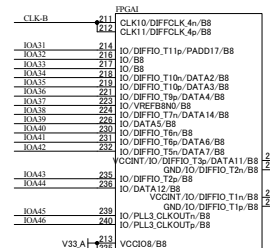
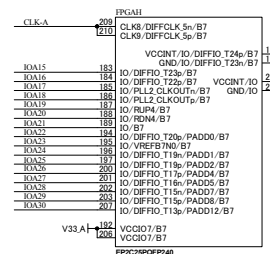
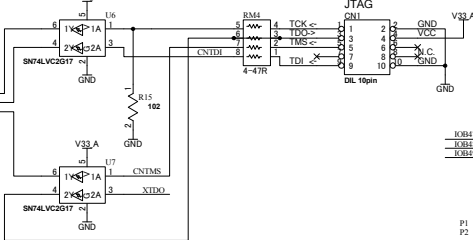
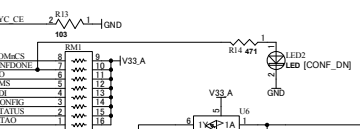
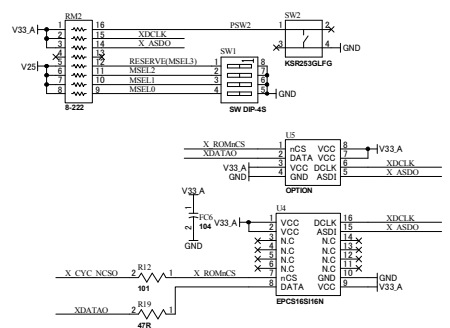
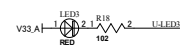
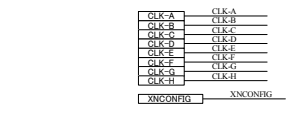
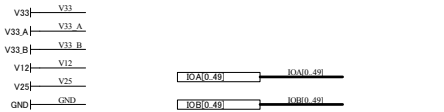


IOAM #P1	IOA[0..49]
IOA[0..49]	IOA[0..49]
CLK-A	CLK-A
CLK-B	CLK-B
CLK-C	CLK-C
CLK-D	CLK-D
CLK-E	CLK-E
CLK-F	CLK-F
CLK-G	CLK-G
CLK-H	CLK-H
XNCONFIG	XNCONFIG



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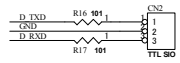
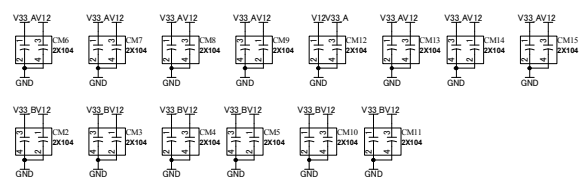
These pins are connected to GND or VCCINT. You need to set them as INPUT.

These pins are connected to GND or VCCINT. You need to set them as INPUT.

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		HuMANDATA LTD. OSAKA JAPAN www.hdl.co.jp/en/(Global) www.hdl.co.jp/(Japan)		Altera CycloneIII Q240 FPGA board		DOC. No. ACM-018	D